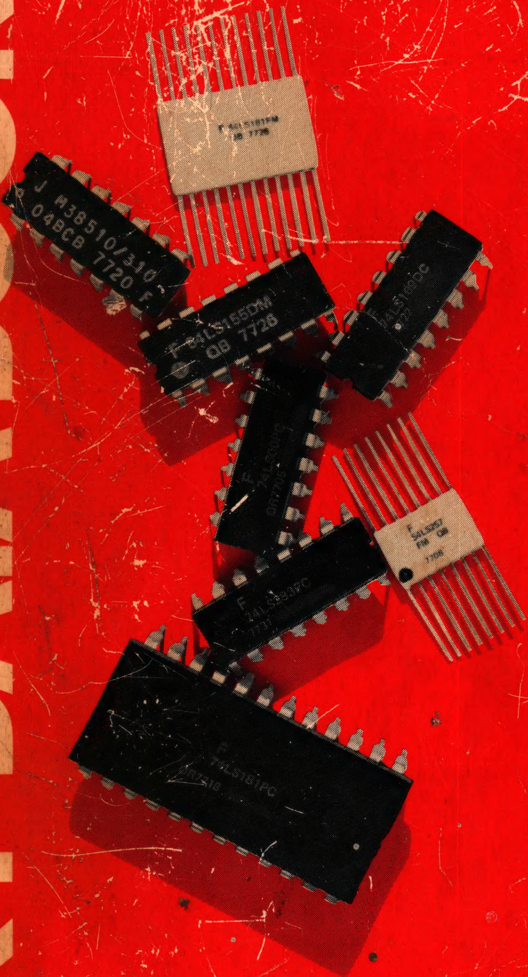
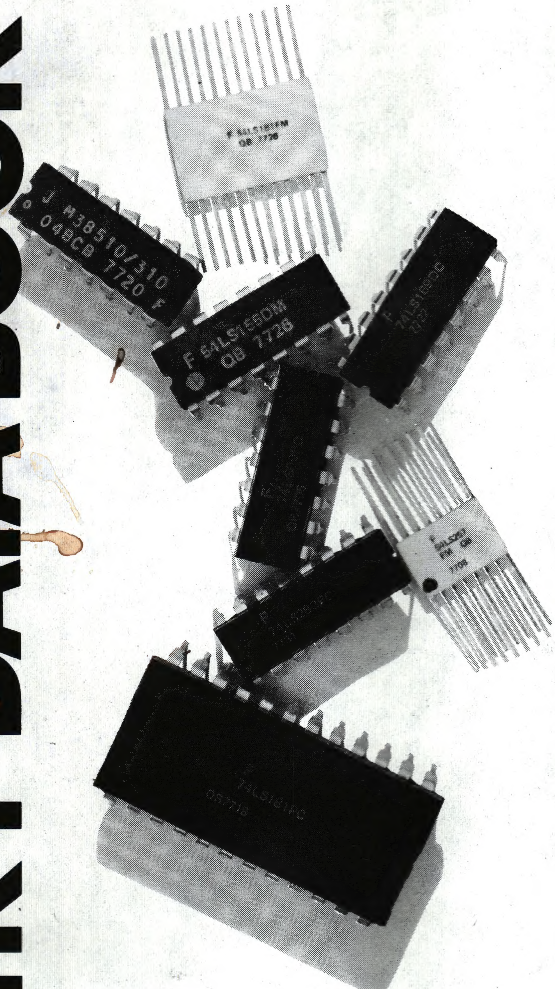
LOW POWER SCHOTTKY DATA BOOK



FAIRCHILD

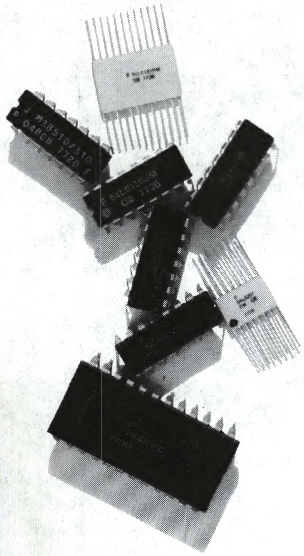
LOW POWER SCHOTTKY DATA BOOK



FAIRCHILD

464 Ellis Street, Mountain View, California 94042

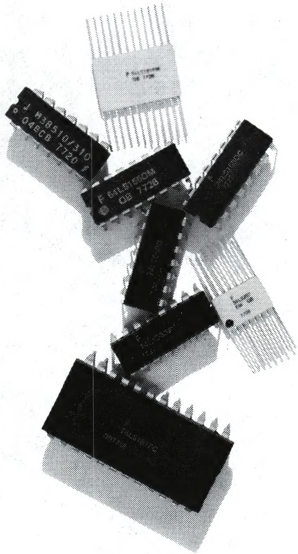
TABLE OF CONTENTS



INTRODUCTION

For many years, TTL has been the most popular digital integrated circuit technology offering an excellent compromise between cost, speed, power consumption and ease of use. As the price of TTL circuits decreased and the average IC complexity increased to MSI (medium scale integration), the cost and size of the power supply and the difficulty of removing the heat dissipated in the TTL circuits became increasingly important factors. Recent improvements in semiconductor processing have made it possible to not only reduce TTL power consumption significantly, but also to improve the speed over that of standard TTL.

Fairchild's Low Power Schottky TTL family combines a power reduction by a factor of five (compared to 7400 TTL) with anti-saturation Schottky diode clamping and advanced processing, using shallower diffusions and higher sheet resistivity to achieve circuit performance better than conventional TTL. With a full complement of popular TTL functions available in LS, Low Power Schottky is destined to become the dominant TTL logic family.



LSTTL circuit features are best understood by examining the LS00 2-input NAND gate *(Figure 2-1)*. The input/output circuits of all LSTTL, including SSI, MSI and MACROLOGIC TTL are almost identical. Although the logic function and basic structure of LS circuits are the same as conventional TTL, there are also significant differences.

INPUT CONFIGURATION. With a few exceptions, LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in *Figure 2-1*. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 10 V and the input breakdown voltage is guaranteed to be 15 V or more. *Figure 2-2* shows the V_{OUT}/V_{IN} transfer function of an LS00 gate. The input threshold is approximately 0.1 V lower than for standard TTL.

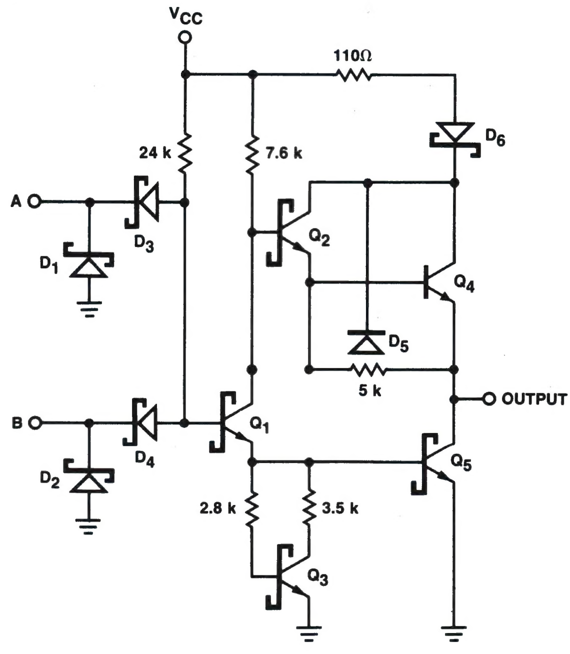


Fig. 2-1
2-INPUT NAND GATE

Another input arrangement often used in MSI has three diodes connected as shown in *Figure 2-3*. This configuration gives a slightly higher input threshold than that of *Figure 2-1*.

A third input configuration that is sometimes used employs a vertical pnp transistor as shown in *Figure 2-4*. This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the pnp input configuration have breakdown voltage ratings greater than 15 V.

A few LS circuits use the traditional emitter inputs and thus have input breakdown ratings of 5.5 V. These circuits are the open-collector gate types LS03, LS05, LS22, LS26 and LS136; flip-flop types LS74, LS109, LS112, LS113 and LS114; and the clock inputs of ripple counter types LS90, LS92, LS93, LS196, LS290, LS293, LS390, LS393 and LS490.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in *Figure 2-1*. These diodes conduct when an input signal goes negative (*Figure 2-5*), which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2 mA and with a duration greater than 500 ns can activate a parasitic lateral npn transistor, which in turn can steal current from internal nodes of the LS circuit and thus cause logic errors.

The effective capacitance of an LSTTL input is 5 pF for DIP and 4 pF for Flatpak. For an input that serves more than one internal function, each additional function adds 1.5 pF.

OUTPUT CONFIGURATION. The output circuitry of LSTTL have several features not found in conventional TTL. A few of these features are discussed below.

Referring to *Figure 2-1*, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (*Figure 2-2*) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

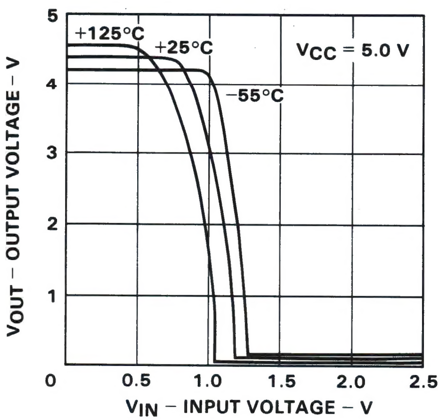


Fig. 2-2
TYPICAL OUTPUT VS INPUT VOLTAGE CHARACTERISTIC

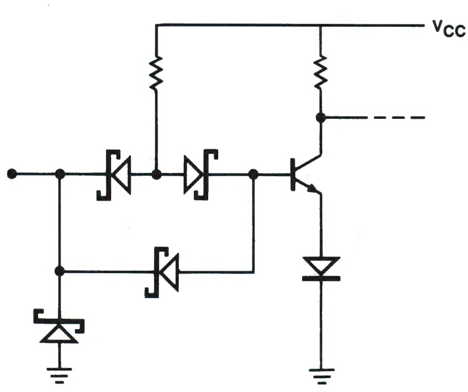


Fig. 2-3
DIODE CLUSTER INPUT

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5 K resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.

As a unique feature, Fairchild LS outputs have a Schottky diode in series with the Darlington collector resistor. This diode allows the output to be pulled substantially higher than V_{CC}, e.g., to +10 V, convenient for interfacing with CMOS. For the same reason, the parasitic diode of the base-return resistor is connected to the Darlington common collector, not to V_{CC}. Some early FSC LS designs – the LS00, LS02, LS04, LS10, LS11, LS20, LS32, LS74, LS109, LS112, LS113 and LS114 – do not have the diode in series with the Darlington collector resistor. These outputs are, therefore, clamped one diode drop above the positive supply voltage V_{CC}.

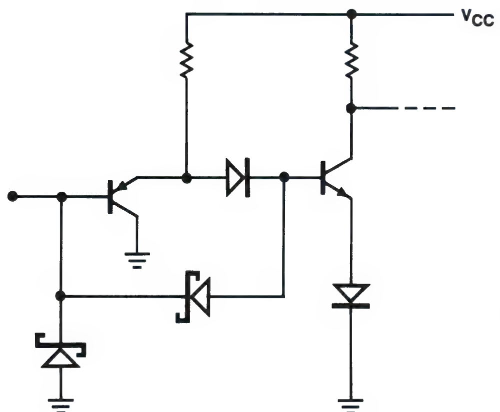


Fig. 2-4
PNP INPUT

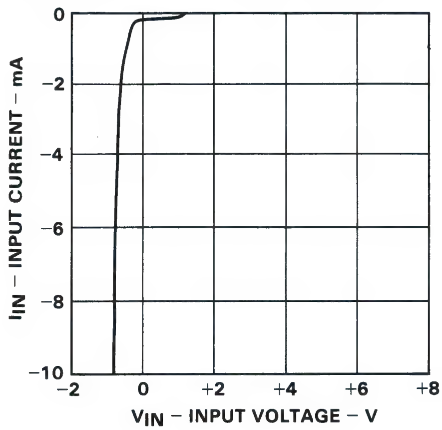


Fig. 2-5
TYPICAL INPUT CURRENT-VOLTAGE CHARACTERISTIC

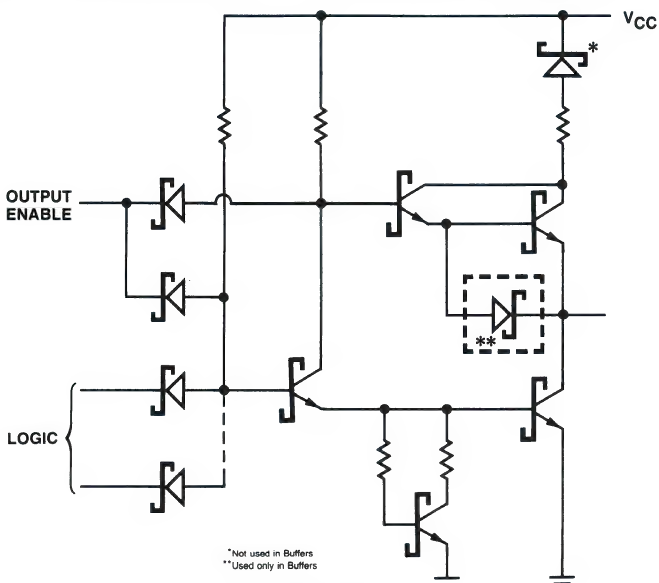


Fig. 2-6
TYPICAL 3-STATE OUTPUT CONTROL

Figure 2-6 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is LOW, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of 2 or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time. *Figure 2-6* also shows that the LS Buffers have a blocking diode in series with the resistor bridging the base-emitter of the pull-up transistor. This serves the same purpose as D6 in *Figure 2-1* – it allows a 3-state Buffer output to be pulled up to 10 volts. Deleting the blocking diode from the Darlington collector return to V_{CC} also allows the Buffer to supply greater pull-up current during an output LOW-to-HIGH transition.

OUTPUT CHARACTERISTICS. *Figure 2-7* shows the LOW-state output characteristics. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition. This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting-edge rate is approximately 0.5 V/ns with a 15 pF load and 0.25 V/ns with a 50 pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$V(t) = V_{OL} + 3.7\left[1 - \exp(-t/T)\right]$$

where $T = 8$ ns for $C_L = 15$ pF and 16 ns for $C_L = 50$ pF

The waveform of a falling output signal resembles that part of a cosine wave between angles of 0° and 180°. Fall times from 90% to 10% are approximately 4.5 ns with a 15 pF load and 8.5 ns with a 50 pF load. Equivalent edge rates are approximately 0.8 and 0.4 V/ns respectively. For analytical purposes, the falling waveform can be approximated by the following.

$$V(t) = V_{OL} + 1.9\,\mu(t)\left[1 + \cos\omega t\right] - 1.9\,\mu(t-a)\left[1 + \cos\omega(t-a)\right]$$

where $\mu(t) = 0$ for $t < 0$ and $\mu(t-a) = 0$ for $t < a$
$= 1$ for $t > 0$ $= 1$ for $t > a$

For t in nanoseconds and $C_L = 15$ pF, $a = 7.5$ ns, $\omega = 0.42$

For $C_L = 50$ pF, $a = 14$ ns, $\omega = 0..23$

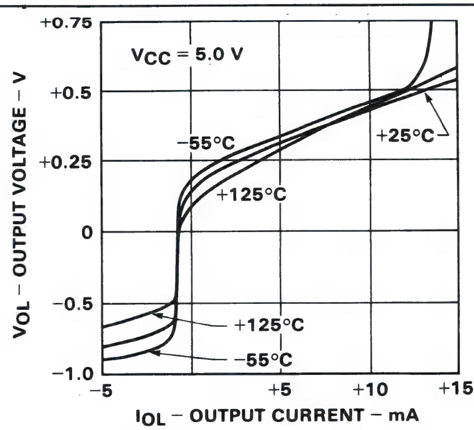


Fig. 2-7 TYPICAL OUTPUT CURRENT-VOLTAGE CHARACTERISTIC

AC SWITCHING CHARACTERISTICS. The average propagation delay of a Low Power Schottky gate is 5 ns at a load of 15 pF as shown in *Figure 2-8*. The delay times increase at an average of 0.08 ns/pF for larger values of capacitance load. These delay times are relatively insensitive to variations in power supply and temperature. The average propagation delay time changes less than 1.0 ns over temperature and less than 0.5 ns with V_{CC} for the military temperature and voltage ranges. (See *Figures 2-10* and *2-11*).

The power versus frequency characteristics of Fairchild's LS family, as shown in *Figure 2-9*, indicate that at operating frequencies above 1 MHz the Low Power Schottky devices are more efficient than CMOS for most applications.

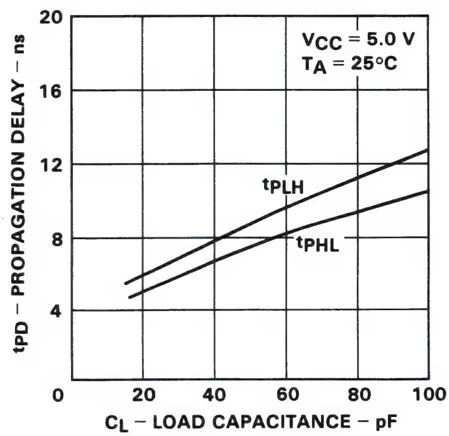


Fig. 2-8

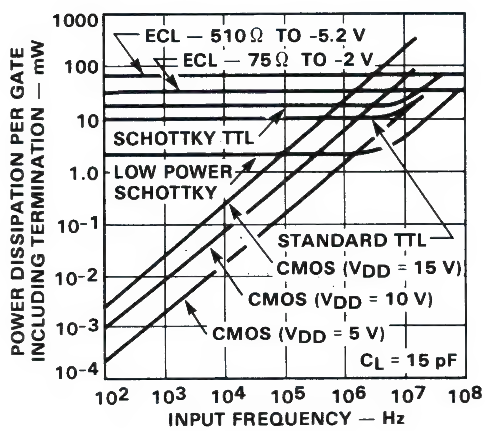


Fig. 2-9

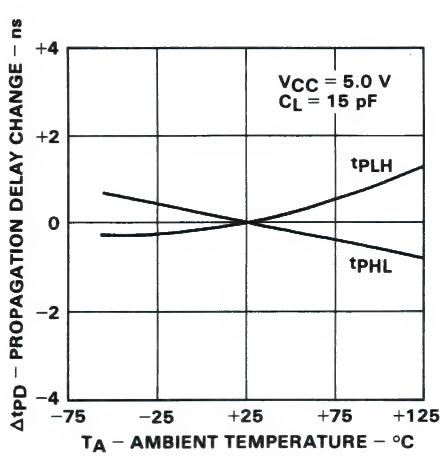


Fig. 2-10

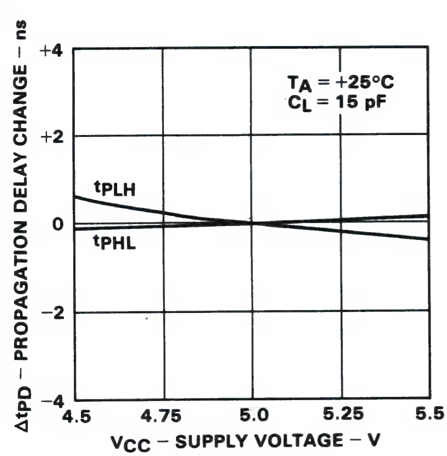
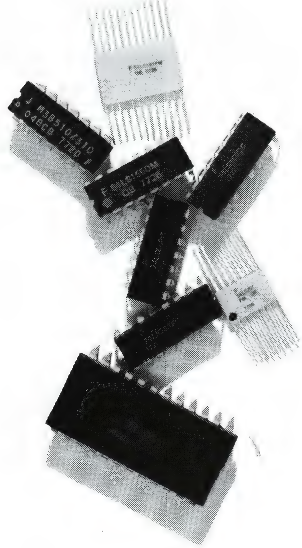


Fig. 2-11



DESIGN CONSIDERATIONS

SUPPLY VOLTAGE AND TEMPERATURE RANGE. The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 70°C. MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

TTL families may be mixed for optimum system design. The following tables specify the worst case noise immunity in mixed systems.

3

Worst Case TTL DC Noise Immunity/Noise Margins

Electrical Characteristics

Item	Symbol	Fairchild TTL Families	Military (−55 to +125°C)				Commercial (0 to 70°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL, 54H/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
8	LPTTL	Low Power TTL, 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
9	STTL	Schottky TTL 54S/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
10	LSTTL	Low Power Schottky TTL 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	300	400	300	mV
HTTL	400	400	300	400	300	mV
LPTTL	500	500	400	500	400	mV
STTL	300	300	200	300	200	mV
LSTTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	500	500	500	500	500	mV
LSTTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	500	500	500	500	500	mV
STTL	300	300	300	300	300	mV
LSTTL	300	300	300	300	300	mV

From "V_{OL}" to V_{IL}"

HIGH Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	700	700	700	700	700	mV
LSTTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

FAN-IN AND FAN-OUT. In order to simplify designing with Fairchild TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA in the HIGH state (logic "1")
1 TTL Unit Load (U.L.) = 1.6 mA in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES – INPUT LOAD

1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\text{ mA}}{1.6\text{ mA}} \text{ or } 0.5 \text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 1 \text{ U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.36\text{ mA}}{1.6\text{mA}} \text{ or } 0.225 \text{ U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 0.5 \text{ U.L.}$$

EXAMPLES – OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\text{ mA}}{1.6\text{ mA}} = 10 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00XC (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\ \text{mA}}{1.6\ \text{mA}} \text{ or } 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in *Table 1.*

TABLE I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP
RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(\text{LOW}) \bullet 1.6\ \mu\text{A}} \qquad R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(\text{HIGH}) \bullet 40\ \mu\text{A}}$$

where:

R_X = External Pull-up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads being Driven
$I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan-out Current of Driving Element
V_{OL} = Output LOW Voltage Level (0.5 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5V}{8\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1	$= 4$
$N_2(HIGH)$	$= 4 \bullet 0.5$ U.L. $= 2$ U.L.
$N_2(LOW)$	$= 4 \bullet 0.25$ U.L. $= 1$ U.L.
I_{OH}	$= 100\ \mu A$
I_{OL}	$= 8$ mA
V_{OL}	$= 0.5$ V
V_{OH}	$= 2.4$ V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}. Most 9LS inputs have a breakdown voltage > 15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1-to-10 kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, where upon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a circumstance that exists any time a transmission line is terminated by an impedance lower than its characteristic impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATABOOK

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} — **Supply current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} — **Input HIGH current** – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} — **Input LOW current** – The current flowing out of an input when a specified LOW voltage is applied.

3

I_{OH} — **Output HIGH current** – The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} — **Output LOW current** – The current flowing into an output which is in the LOW state.

I_{OS} — **Output short-circuit current** – The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).

I_{OZH} — **Output off current HIGH** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} — **Output off current LOW** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, −10 V is greater than −1.0 V).

V_{CC} — **Supply voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(MAX)}$ — **Input clamp diode voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} — **Input HIGH voltage** – The range of input voltages that represents a logic HIGH in the system.

$V_{IH(MIN)}$ — **Minimum input HIGH voltage** – The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} — **Input LOW voltage** – The range of input voltages that represents a logic LOW in the system.

$V_{IL(MAX)}$ — **Maximum input LOW voltage** – The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ — **Output HIGH voltage** – The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ — **Output LOW Voltage** – The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{T+} — **Positive-going threshold voltage** – The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

V_{T-} — **Negative-going threshold voltage** – The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS

f_{MAX} **Toggle frequency/operating frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse width** – The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.

t_h **Hold time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

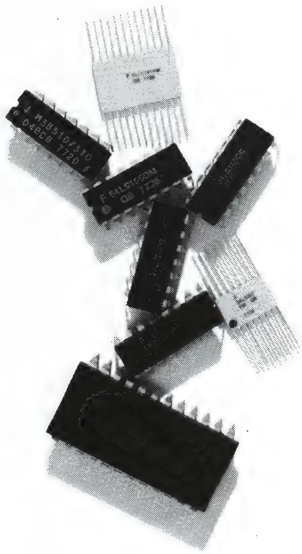
t_{PHZ} **Output disable time (of a 3-state output) from HIGH level** – The time between the 1.3 V level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.

t_{PLZ} **Output disable time (of a 3-state output) from LOW level** – The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.

t_{PZH} **Output enable time (of a 3-state output) to a HIGH level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.

t_{PZL} **Output enable time (of a 3-state output) to a LOW level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.

t_{rec} **Recovery time** – The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.



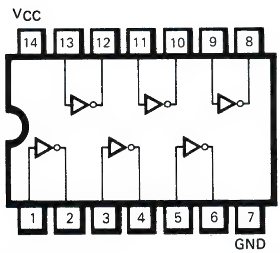
NUMERICAL INDEX OF DEVICES

*DATA SHEET provides tentative information on a new product. Fairchild Semiconductor reserves the right to change specifications for this product in any manner without notice.

SSI SELECTOR AND REPLACEMENT GUIDE

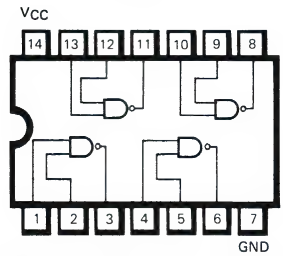
Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol
NAND Gates					
Hex Inverters	54LS/74LS04	54/7404	54H/74H04	54S/74S04	D-1
Hex Inverters (o. c.)	54LS/74LS05	54/7405	54H/74H05	54S/74S05	D-1
Hex Schmitt Trigger	54LS/74LS14	54/7414			D-1
Quad 2-Input	54LS/74LS00	54/7400	54H/74H00	54S/74S00	D-2
Quad 2-Input (o. c.)	54LS/74LS03	54/7403		54S/74S03	D-2
Quad 2-Input (48 mA)	54LS/74LS37	54/7437			D-2
Quad 2-Input (o. c. 48 mA)	54LS/74LS38	54/7438			D-2
Quad 2-Input (o. c. 15 V)	54LS/74LS26				D-2
Quad 2-Input Schmitt	54LS/74LS132	54/74132		54S/74S132	D-2
Triple 3-Input	54LS/74LS10	54/7410	54H/74H10	54S/74S10	D-3
Dual 4-Input Schmitt	54LS/74LS13	54/7413			D-4
Dual 4-Input	54LS/74LS20	54/7420	54H/74H20	54S/74S20	D-4
Dual 4-Input (o. c.)	54LS/74LS22	54/7422	54H/74H22	54S/74S22	D-4
Dual 4-Input Buffer	54LS/74LS40	54/7440	54H/74H40	54S/74S40	D-4
8-Input	54LS/74LS30	54/7430	54H/74H30	54S/74S30	D-5
13-Input	54LS/74LS133			54S/74S133	D-6

D1



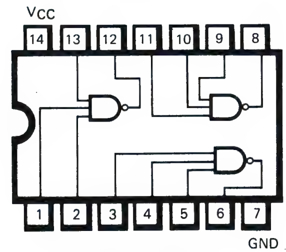
54LS/74LS04, 54LS/74LS05, 54LS/74LS14

D2



54LS/74LS00, 54LS/74LS03 54LS/74LS37, 54LS/74LS38 54LS/74LS26 54LS/74LS132

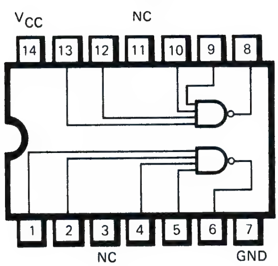
D3



54LS/74LS10

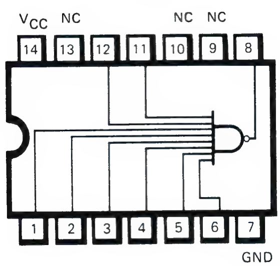
4

D4



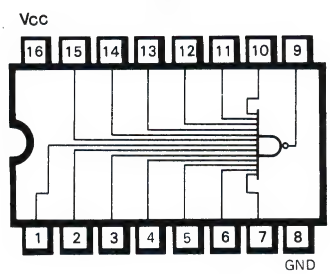
54LS/74LS20 54LS/74LS22, 54LS/74LS40 54LS/74LS13

D5



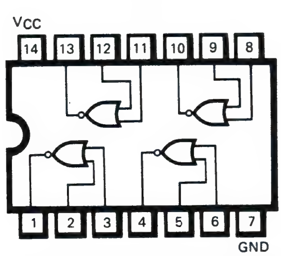
54LS/74LS30

D6



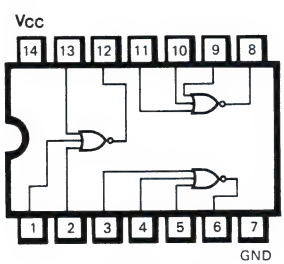
54LS/74LS133

D7



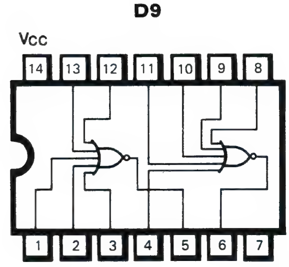
54LS/74LS02, 54LS/74LS28 54LS/74LS33

D8



54LS/74LS27

D9

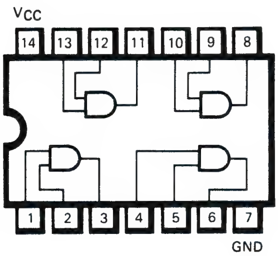


54LS/74LS260

SSI SELECTOR AND REPLACEMENT GUIDE

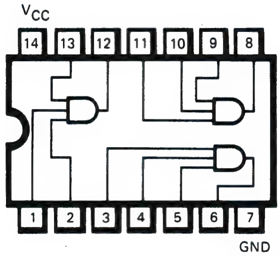
Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol
NOR Gates					
Quad 2-Input	54LS/74LS02	54/7402		54S/74S02	D-7
Quad 2-Input Buffer	54LS/74LS28				D-7
Quad 2-Input (o. c.)	54LS/74LS33				D-7
Triple 3-Input	54LS/74LS27	54/7427			D-8
Dual 5-Input	54LS/74LS260			54S/74S260	D-9
AND Gates					
Quad 2-Input	54LS/74LS08	54/7408	54H/74H08	54S/74S08	D-10
Quad 2-Input (o. c.)	54LS/74LS09	54/7409	54H/74H09	54S/74S09	D-10
Triple 3-Input	54LS/74LS11	54/7411	54H/74H11	54S/74S11	D-11
Triple 3-Input (o. c.)	54LS/74LS115		54H/74H15	54S/74S15	D-11
Dual 4-Input	54LS/74LS21	54/7421	54H/74H21	54S/74S21	D-12
OR Gates					
Dual 2-Input	54LS/74LS32	54/7432		54S/74S32	D-13
Exclusive OR Gate					
Quad 2-Input	54LS/74LS86	54/7486		54S/74S86	D-14
Quad 2-Input	54LS/74LS386				D-15
Quad 2-Input (o. c)	54LS/74LS136				D-14
Exclusive NOR Gate					
Quad 2-Input (o. c.)	54LS/74LS266	9386 (8242)			D-16

D10



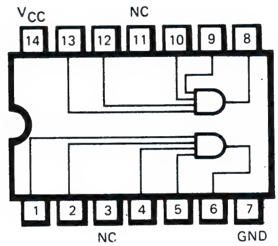
54LS/74LS08
54LS/74LS09

D11



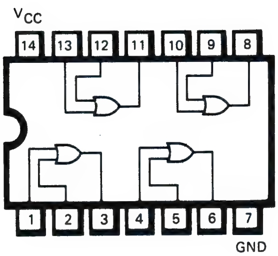
54LS/74LS11
54LS/74LS15

D12



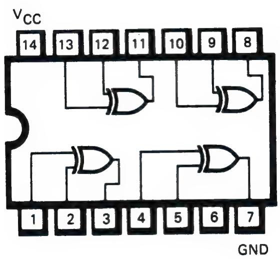
54LS/74LS21

D13



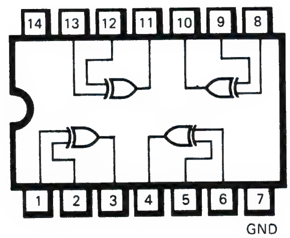
54LS/74LS32

D14



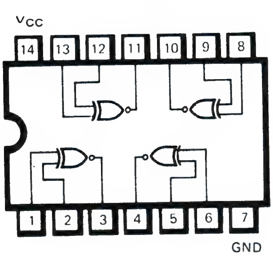
54LS/74LS86
54LS/74LS136

D15



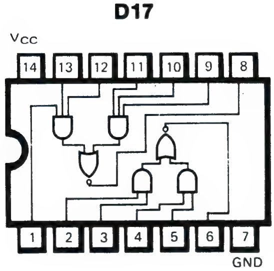
54LS/74LS386

D16



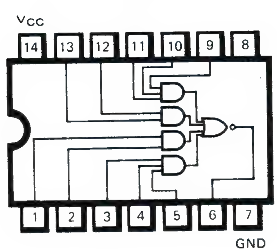
54LS/74LS266

D17



54LS/74LS51

D18



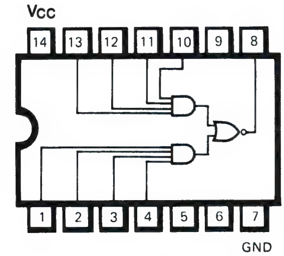
54LS/74LS54

4

SSI SELECTOR AND REPLACEMENT GUIDE

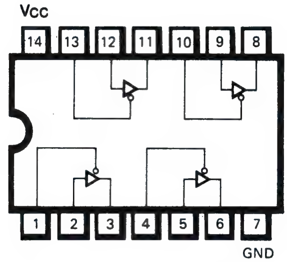
Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol
AND-OR-INVERT GATES					
Dual 2-2-Input	54LS/74LS51	54/7451	54H/74H51	54S/74S51	D-17
2-2-3-3-Input	54LS/74LS54	—	—	—	D-18
4-4-Input	54LS/74LS55	—	—	—	D-19
BUFFERS (3-STATE)		—	—	—	
Quad 3-State LOW Enable	54LS/74LS125	54/74125	—	—	D-20
Quad 3-State HIGH Enable	54LS/74LS126	54/74126	—	—	D-21
Hex Buffer 3-State Common Enable	54LS/74LS365	—	—	—	D-22
Hex Inverting 3-State Common Enable	54LS/74LS366	—	—	—	D-23
Hex Buffer 4-Bit & 2-Bit	54LS/74LS367	—	—	—	D-24
Hex Inverting 4 Bit-&-2 Bit	54LS/74LS368	—	—	—	D-25

D19



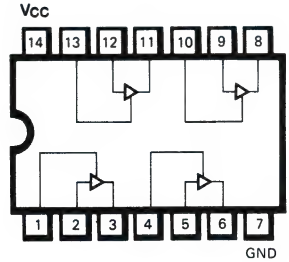
54LS/74LS55

D20



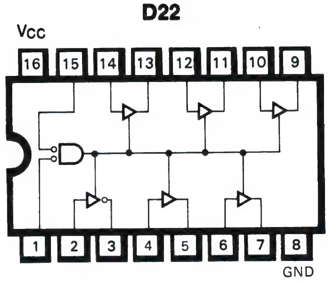
54LS/74LS125

D21



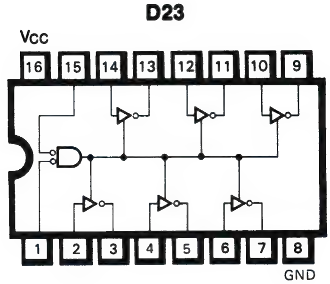
54LS/74LS126

D22



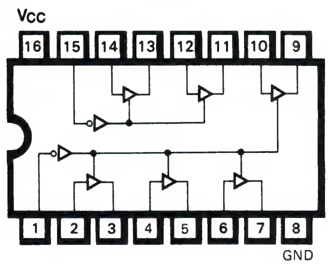
54LS/74LS365

D23



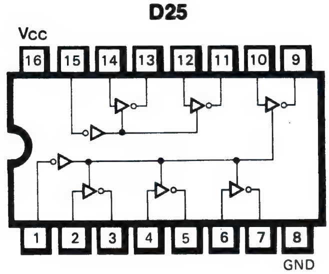
54LS/74LS366

D24



54LS/74LS367

D25



54LS/74LS368

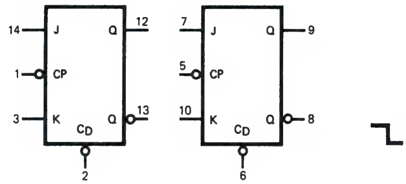
4

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol
DUAL FLIP-FLOPS					
Dual JK	(54LS/74LS73)	(54/7473)	54H/74H73		D-26
Dual JK	54LS/74LS76	54/7476	54H/74H76		D-28
Dual JK	54LS/74LS78		54H/74H78		D-29
Dual JK	54LS/74LS107	54/74107			D-30
Dual JK	54LS/74LS109	9024		54S/74S109	D-31
Dual JK	54LS/74LS112			54S/74S112	D-32
Dual JK	54LS/74LS113			54S74S113	D-33
Dual JK	54LS/74LS114			54S/74S114	D-34
Dual D	54LS/74LS74	54/7474	54H/74H74	54S/74S74	D-27

SSI FLIP-FLOP LOGIC DIAGRAM

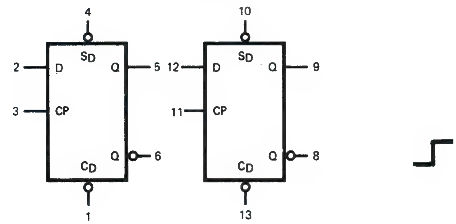
D26



VCC = Pin 4
GND = Pin 11

54LS/74LS73

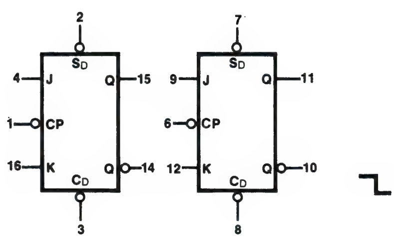
D27



VCC = Pin 14
GND = Pin 7

54LS/74LS74

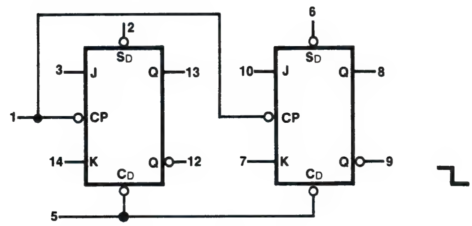
D28



VCC = Pin 5
GND = Pin 13

54LS/74LS76

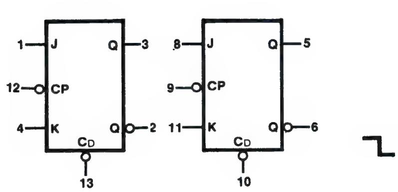
D29



VCC = Pin 4
GND = Pin 11

54LS/74LS78

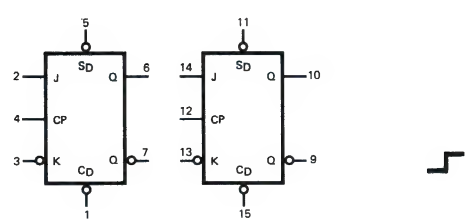
D30



VCC = Pin 14
GND = Pin 7

54LS/74LS107

D31

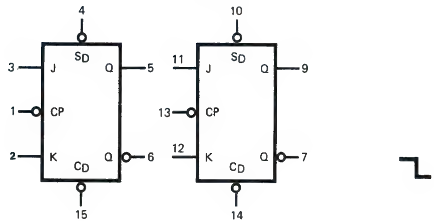


VCC = Pin 16
GND = Pin 8

54LS/74LS109

4

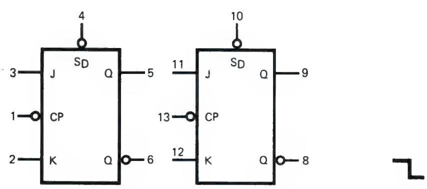
D32



Vcc = Pin 16
GND = Pin 8

54LS/74LS112

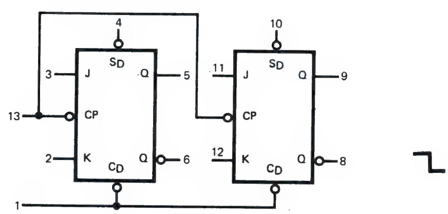
D33



Vcc = Pin 14
GND = Pin 7

54LS/74LS113

D34



Vcc = Pin 14
GND = Pin 7

54LS/74LS114

MSI SELECTOR GUIDE BY FUNCTION

Counters

A= Asynchronous S = Synchronous

Function	DEVICE NO.	Modulo	Parallel Load	Clock Transition	Max Clock Rate MHz (typ)	Clock to Q Output Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Asynchronous	54LS/74LS90	2x5		↓	50	33	45	
Asynchronous	54LS/74LS92	2x6		↓	50	33	45	
Asynchronous	54LS/74LS93	2x8		↓	50	46	45	
Asynchronous	54LS/74LS196	2x5	A	↓	60	48	60	
Asynchronous	54LS/74LS197	2x8	A	↓	70	60	60	
Asynchronous	54LS/74LS290	2x5		↓	50	10	45	
Asynchronous	54LS/74LS293	2x8		↓	50	10	45	
Asynchronous	54LS/74LS390	2x5 2x5		↓	50	10	100	
Asynchronous	54LS/74LS343	2x8 2x8		↓	50	10	100	
Asynchronous	54LS/74LS490	2x5 2x5		↓	50	6	100	
Synchronous	54LS/74LS160	10 Presettable	S	↑	45	15	95	
Synchronous	54LS/74LS161	16 Presettable	S	↑	45	15	95	
Synchronous	54LS/74LS162	10 Presettable	S	↑	45	15	95	
Synchronous	54LS/74LS163	16 Presettable	S	↑	45	15	95	
Up/Down	54LS/74LS168	10 Presettable	S	↑	32	15	100	
Up/Down	54LS/74LS169	16 Presettable	S	↑	32	15	100	
Up/Down	54LS/74LS190	10	A	↑	40	20	90	
Up/Down	54LS/74LS191	16	A	↑	40	20	90	
Up/Down	54LS/74LS192	10	A	↑	40	30	85	
Up/Down	54LS/74LS193	16	A	↑	40	30	85	

MSI SELECTOR GUIDE BY FUNCTION

ARITHMETIC OPERATORS

(CLA = Carry Lookahead)

Function	Device No.	Description	No. of Bits	Typical t_{pd} ns	Power Dissipation mW (typ)
Adder	54LS/74LS83A	Full Binary 4-Bit w/Carry	4	15	95
Adder	54LS/74LS283	Full Binary 4-Bit w/Carry	4	15	95
Arithmetic Logic Unit	54LS/74LS181	ALU with External CLA	4	20	105
Carry Lookahead Generator	54LS/74LS182	Carry Lookahead	—	—	—

MSI SELECTOR GUIDE BY FUNCTION

DECODER/DEMULTIPLEXERS

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	Device No.	Address Inputs	Active LOW Enable	Active LOW Outputs	Open Collector Output Voltage	Address Delay ns (typ)	Enable Delay ns (typ)	Power Dissipation mW (typ)	Fan-out (UL)
Dual 1-of-4	54LS/74LS139	2+2	1+1	4+4	—	22	19	34	5
Dual 1-of-4	54LS/74LS155	2	2+2	4+4	—	18	15	30	5
Dual 1-of-4	54LS/74LS156	2	2+2	4+4	5.5 V	33	26	31	5
Dual 1-of-4	54LS/74LS256	2+2	1	4+4	—	30	19	60	5
BCD to 7-Segment	54LS/74LS47	4	—	7	15 V	50	—	35	15
BCD to 7-Segment	54LS/74LS48	4	—	7	5.5 V	50	—	125	4
BCD to 7-Segment	54LS/74LS49	4	—	7	5.5 V	50	—	40	5
BCD to 7-Segment	54LS/74LS247	4	—	7	15 V	50	—	35	15
BCD to 7-Segment	54LS/74LS248	4	—	7	5.5 V	50	—	125	4
BCD to 7-Segment	54LS/74LS249	4	—		5.5 V	50	—	40	5
1-of-8	54LS/74LS259	3	1	8	—	30	19	60	5
1-of-8	54LS/74LS42	3	1	8	—	17	17	35	5
1-of-8	54LS/74LS138	3	3	8	—	22	21	34	5
1-of-10	54LS/74LS42	4(BCD)	—	10	—	17	—	35	5

LATCHES AND FLIP-FLOPS

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	Device No.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/ Clock Pulse Width ns (typ)	Enable/Clock to Q Delay ns (typ)	Data to Q Delay ns (typ)	Power Dissipation mW (typ)
4-Bit RS Latch	54LS/74LS279	4x(RS)	—	—	—	—	14	19
4-Bit D Latch	54LS/74LS75	4xD	—	2(L)	10	15	15	32
4-Bit D Latch	54LS/74LS77	4xD	—	2(L)	10	15	15	32
4-Bit D Latch	54LS/74LS197	4xD	L	1(L)	20	28	24	60
4-Bit D Latch	54LS/74LS375	4xD	—	2(L)	10	15	15	32
8-Bit D Latch	54LS/74LS373	8xD	—	1(H)	10	14	10	120
8-Bit D Latch	54LS/74LS573	8xD	—	1(H)	10	14	10	120
Dual 4-Bit Addressable Latch	54LS/74LS256	1xD	L	1(L) 2 Add Bits	11	18	28	70
8-Bit Addressable Latch	54LS/74LS259	1xD	L	1(L) 3 Add Bits	11	18	28	70
4-Bit D Flip-Flop	54LS/74LS175	4xD	L	1(↑)	20	21	—	55
4-Bit D Flip-Flop	54LS/74LS298	4x2	—	1(↓)	20	20	—	65
4-Bit D Flip-Flop	54LS/74LS174	6	L	1(↑)	20	21	—	80
4x4 Register File	54LS/74LS170	4xD	—	2	25	—	26	125
4x4 Register File (3-State)	54LS/74LS670	4xD	—	2	25	—	24	150
Quad D Flip-Flop	54LS/74LS379	4xD	—	1(↑)	20	21	—	—
Hex D Flip-Flop	54LS/74LS378	6xD	—	1(↑)	20	21	—	—
Octal D Flip-Flop	54LS/74LS377	8xD	—	1(↑)	20	21	—	—
Octal D Flip-Flop	54LS/74LS273	8xD	L	1(↑)	15	17	—	85
Octal D Flip-Flop	54LS/74LS374	8xD	—	1(↑)	12	22	—	135
Octal D Flip-Flop	54LS/74LS574	8xD	—	1(↑)	12	22	—	135

MSI SELECTOR GUIDE BY FUNCTION

MULTIPLEXERS
Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

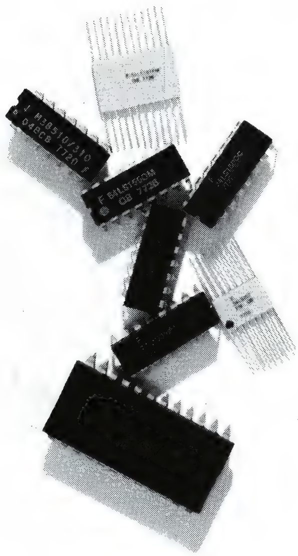
Function	Device No.	Enable Inputs	True Output	Complement Output	Select Delay ns (typ)	Enable Delay ns (typ)	Data Delay ns (typ)	Power Dissipation mW (typ)	Fan-Out (UL)
Quad 2-Input	54LS/74LS157	1	x	—	18	14	9	49	5
Quad 2-Input	54LS/74LS158	1	—	x	16	12	7	24	5
Quad 2-Input	54LS/74LS257	1	3-State	—	14	16	12	50	5
Quad 2-Input	54LS/74LS258	1	—	3-State	12	16	10	35	5
Quad 2-Input	54LS/74LS298	Clocked (edge-trigger)	x Latched	—	—	20	—	65	5
Quad 2-Input	54LS/74LS398	Clocked (edge-trigger)	x Latched	x Latched	—	20	—	37	5
Quad 2-Input	54LS/74LS399	Clocked (edge-trigger)	x Latched	—	—	20	—	37	5
Dual 4-Input	54LS/74LS153	2	x	—	18	16	10	31	5
Dual 4-Input	54LS/74LS253	2	3-State	—	18	16	10	43	5
Dual 4-Input	54LS/74LS352	2	—	x	17	15	8	30	5
Dual 4-Input	54LS/74LS353	2	—	3-State	20	12	10	43	5
8-Input	54LS/74LS151	1	x	x	28	25	18	30	5
8-Input	54LS/74LS251	1	3-State	3-State	29	21	18	33	5
8-Input	54LS/74LS152	—	—	x	22	—	11	28	5

MSI SELECTOR GUIDE BY FUNCTION

REGISTERS

A = Asynchronous, S= Synchronous

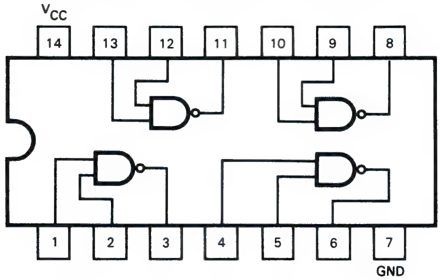
Function	Device No.	No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	Max Clock Freq MHz (typ)	Clock to Output Delay ns (typ)	Power Dissipation mW (typ)
Parallel-In/Parallel-out Shift Right	54LS/74LS95B	4	D	4S	↓	36	20	65
Parallel-in/Parallel-out Shift Right	54LS/74LS195	4	J, K	4S	↑	39	17	70
Parallel-in/Parallel-out Shift Right	54LS/74LS295	4	D	4S	↑	28	40	75
Parallel-in/Parallel-out Shift Right	54LS/74LS395	4	D	4S	—	45	20	95
Parallel-in/Parallel-out Bi-Directional	54LS/74LS194	4	DR, DL	4S	↑	36	16	75
Parallel-in/Parallel-out Bi-Directional	54LS/74LS299	8	D	8S	↑	40	15	175
Parallel-in/Parallel-out Bi-Directional	54LS/74LS323	8	D	8S	↑	40	15	175
Serial-in/Parallel-out	54LS/74LS164	8	2D	—	↑	18	50	95
Serial-in/Parallel-out	54LS/74LS502	8	D	—	↑	25	18	325
Parallel-in/Parallel-out	54LS/74LS174	6	—	6S	↑	40	21	65
Parallel-in/Parallel-out	54LS/74LS175	4	—	4S	↑	40	21	45
Parallel-in/Parallel-out	54LS/74LS298	4	—	2D MUX	↓	30	21	65
Parallel-in/Parallel-out	54LS/74LS273	8	—	8S	↑	45	18	85
Parallel-in/Parallel-out	54LS/74LS374	8	—	8S	↑	55	20	135
Parallel-in/Parallel-out	54LS/74LS377	8	—	8S	↑	45	18	85
Parallel-in/Parallel-out	54LS/74LS378	6	—	6S	↑	45	20	65
Parallel-in/Parallel-out	54LS/74LS379	4	—	4S	↑	45	15	75
Parallel-in/Parallel-out	54LS/74LS398	4	—	2D MUX	↑	35	20	37
Parallel-in/Parallel-out	54LS/74LS399	4	—	2D MUX	↑	35	20	37
Parallel-in/Parallel-out	54LS/74LS574	8	—	8S	↑	55	20	135
Multiport Registers	54LS/74LS170	16	—	4A	↓	—	25	125
Multiport Registers	54LS/74LS670	16	—	4A	↓	—	30	150
Successive Approximation Register	54LS/74LS502	8	D	—	↑	25	18	325



F54LS/74LS00

QUAD 2-INPUT NAND GATE

CONNECTION AND LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS00XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS00XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

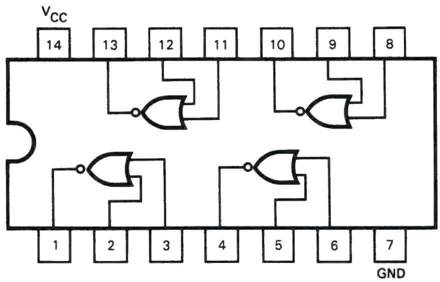
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS02

QUAD 2-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS02XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS02XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.6	3.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	5.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

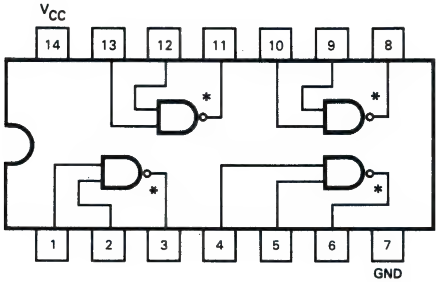
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS03

QUAD 2-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS03XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS03XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

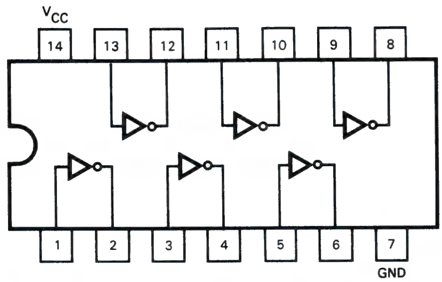
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

F54LS/74LS04
HEX INVERTER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS04XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS04XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

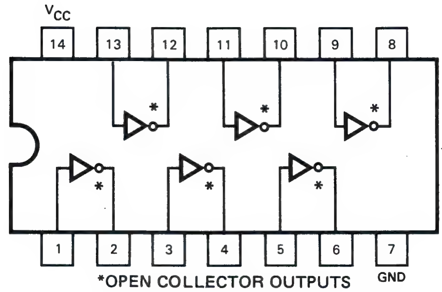
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

F54LS/74LS05

HEX INVERTER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS05XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS05XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

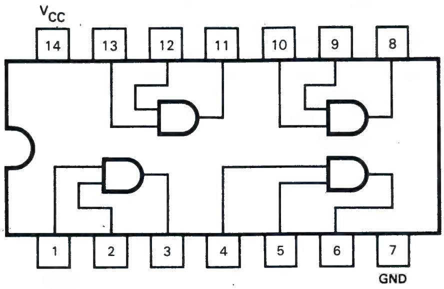
AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.

F54LS/74LS08

QUAD 2-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS08XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS08XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

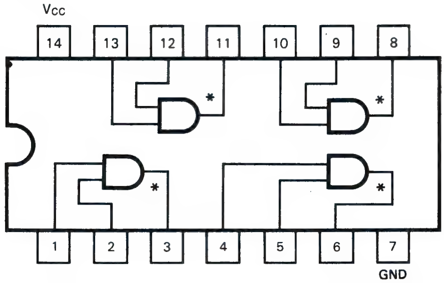
AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		7.5	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS09

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS09XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS09XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

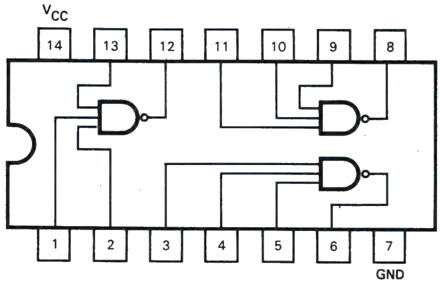
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

F54LS/74LS10

TRIPLE 3-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS10XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS10XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.6	1.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.8	3.3	mA	V_{CC} = MAX, Inputs Open

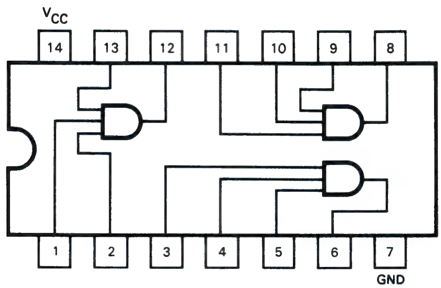
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

F54LS/74LS11

TRIPLE 3-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS11XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS11XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

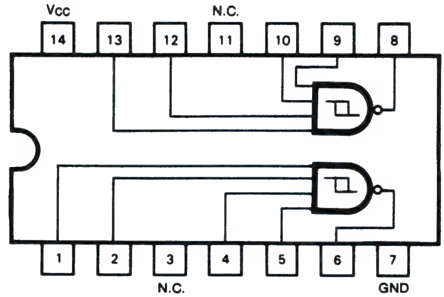
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	4.0	8.5	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.5	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS13

DUAL 4-INPUT SCHMITT TRIGGER



DESCRIPTION — The 54LS/74LS13 contains two 4-Input NAND Gates that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND gates.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drive a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

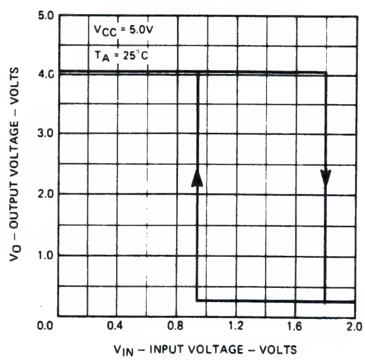


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

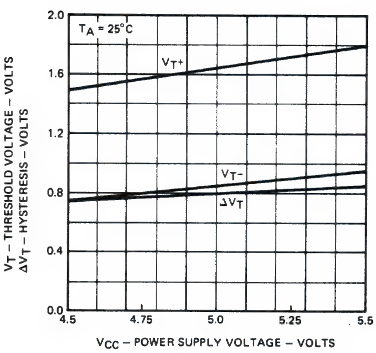


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

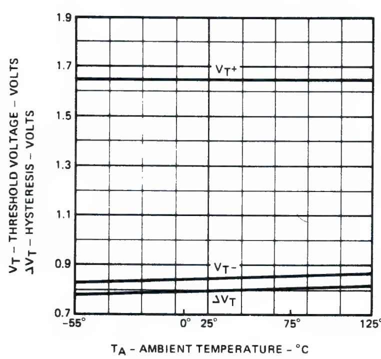


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS13XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS13XC	4.75V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

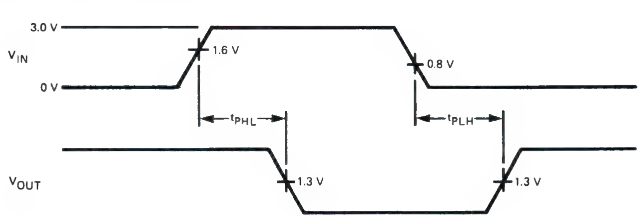
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage		1.5	1.8	2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage		0.6	.95	1.1	V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			8.6	16	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			12	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V

AC CHARACTERISTICS: T_A = 25° C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Input to Output			22	ns	V_{CC} = 5.0 V
t_{PHL}	Propagation Delay, Input to Output			22	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



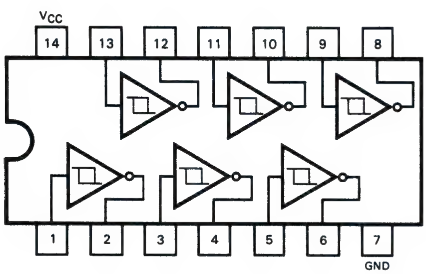
F54LS/74LS14

HEX SCHMITT TRIGGER INVERTER

DESCRIPTION — The 54LS/74LS14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

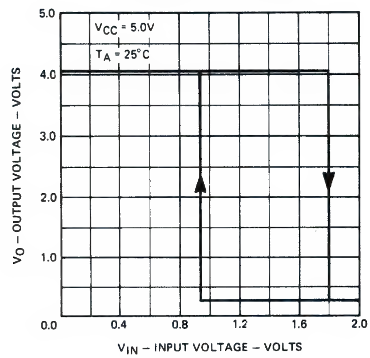


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
POWER SUPPLY VOLTAGE

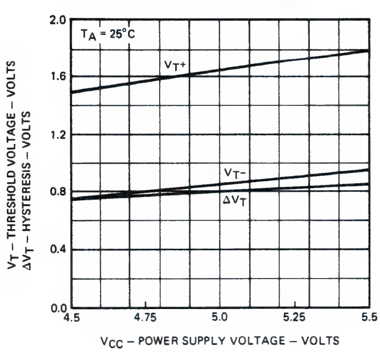


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
TEMPERATURE

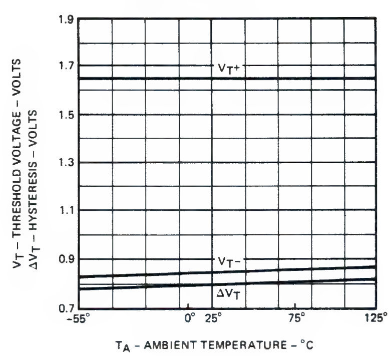


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS14XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS14XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

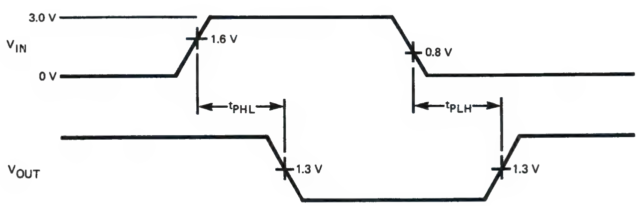
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage		1.5	1.8	2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage		0.6	0.95	1.1	V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			8.6	16	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			12	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V

AC CHARACTERISTICS: T_A = 25°C

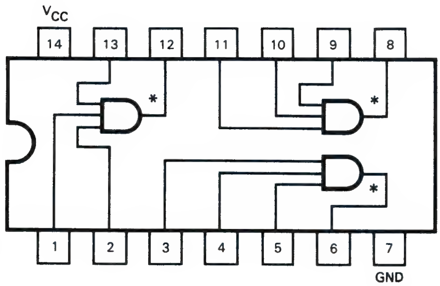
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Input to Output			22	ns	V_{CC} = 5.0 V
t_{PHL}	Propagation Delay, Input to Output			27	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



F54LS/74LS15

TRIPLE 3-INPUT AND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS15XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS15XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

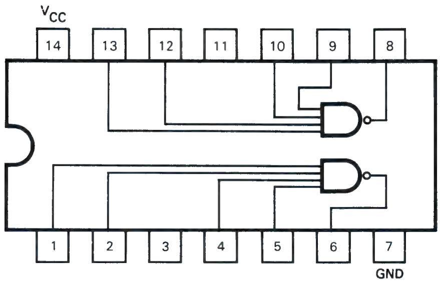
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	7.0	13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	5.0	10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

F54LS/74LS20

DUAL 4-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS20XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS20XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

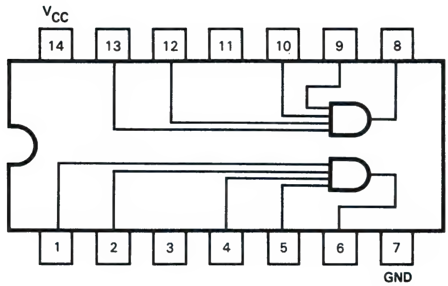
SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	8.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS21
DUAL 4-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS21XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS21XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, $V_{IN} = V_{IH}$
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, $V_{IN} = V_{IL}$
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, $V_{IN} = V_{IL}$
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			2.2	4.4	mA	V_{CC} = MAX, V_{IN} = 0 V

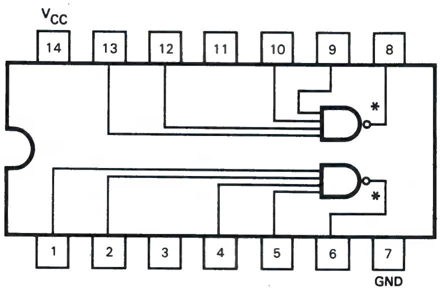
AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

F54LS/74LS22

DUAL 4-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS22XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS22XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

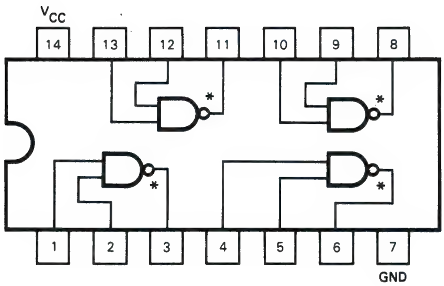
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

F54LS/74LS26

QUAD 2-INPUT NAND BUFFER



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS26XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS26XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				-0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

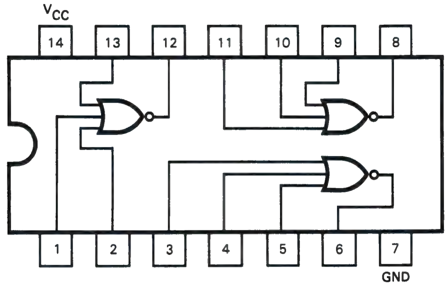
AC CHARACTERISTICS: T_A = 25° C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 k

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.

F54LS/74LS27

TRIPLE 3-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS27XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS27XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.0	4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.4	6.8	mA	V_{CC} = MAX, Inputs Open

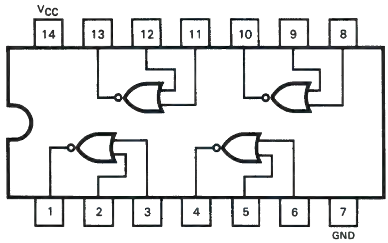
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS28

QUAD 2-INPUT NOR BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS28XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS28XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = Package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM XC			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode			0.85	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM XC	2.5 2.7	3.06		V	I_{OH} = −1.2 mA V_{CC} = MIN, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC XC		0.22 0.26	0.4 0.5	V	I_{OL} = 12 mA I_{OL} = 24 mA V_{CC} = MIN, V_{IN} = V_{IH}
I_{IH}	Input HIGH Current			0.1 0.1	20 100	μA μA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current			1.7	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short-Circuit Current		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current Input HIGH			2.1	3.6	mA	V_{CC} = MAX
I_{CCL}	Supply Current Input LOW			11	13.8	mA	V_{CC} = MAX

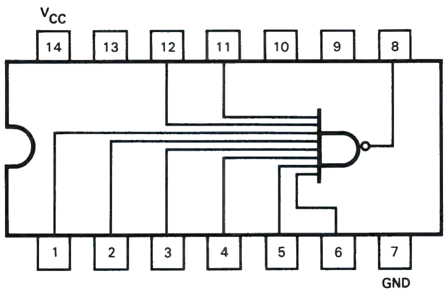
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Propagation Delay		8.5	24	ns	C_L = 50 pF, RL = 667 Ω
t_{PHL}	Propagation Delay		10.5	24	ns	Vcc = 5.0 V

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS30

8-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS30XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS30XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

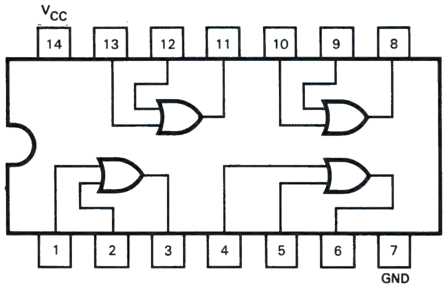
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		6.5	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		12.5	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS32

QUAD 2-INPUT OR GATE

3



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS32XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS32XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA, $V_{IN} = V_{IH}$
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, $V_{IN} = V_{IL}$
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, $V_{IN} = V_{IL}$
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			3.1	6.2	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.9	9.8	mA	V_{CC} = MAX, V_{IN} = 0 V

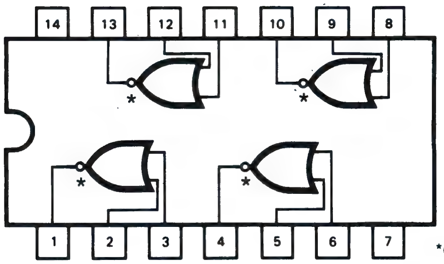
AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS33

QUAD 2-INPUT NOR BUFFER OPEN COLLECTOR



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS33XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS33XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F = Flatpak, D = Ceramic Dip, P = Plastic Dip

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN}, = -18 mA
V_{OH}	Output HIGH Voltage	XM, XC	2.7	3.4			V_{CC} = MIN, I_{OH} -400 μA, $V_{IN} = V_{IL}$
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	V_{CC} = MIN, I_{OL}, = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL}, = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			0.1	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2	3.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			10	13.8	mA	V_{CC} = MAX, Inputs Open

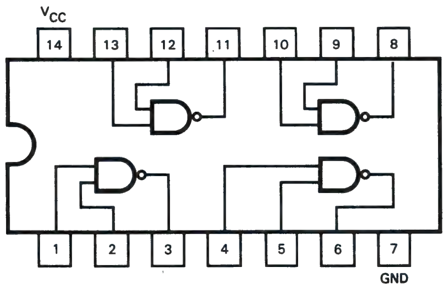
AC CHARACTERISTICS: (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		11	18	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		14	22	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS37

QUAD 2-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS37XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS37XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

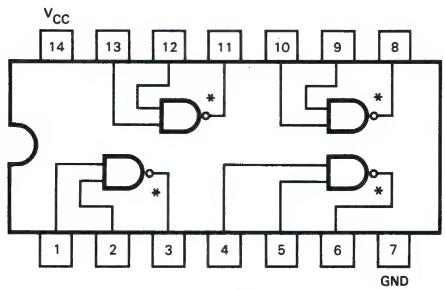
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	20	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS38

QUAD 2-INPUT NAND BUFFER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS38XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS38XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

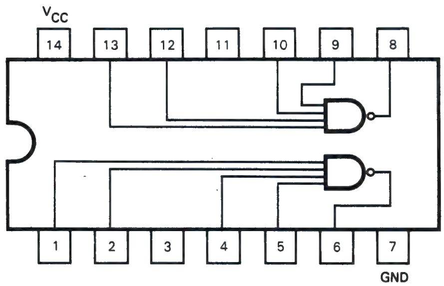
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		14	22	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

F54LS/74LS40

DUAL 4-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS40XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS40XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.45	1.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.0	6.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	24	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		20	24	ns	C_L = 45 pF, R_L = 667 Ω

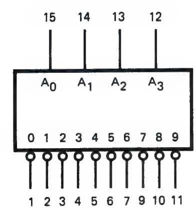
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

F54LS/74LS42
ONE-OF-TEN DECODER

DESCRIPTION — The 54LS/74LS42 is a MSI Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

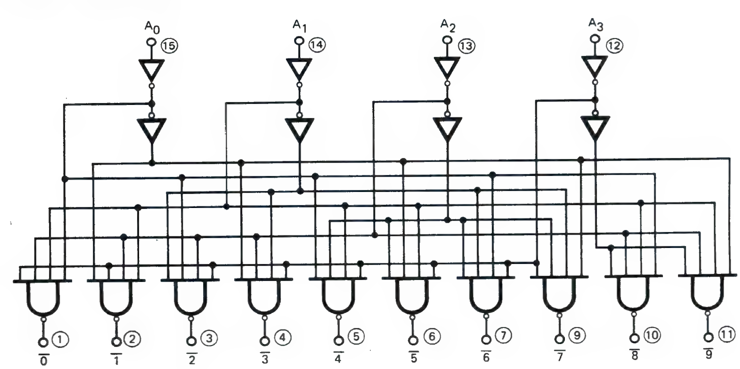
5

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

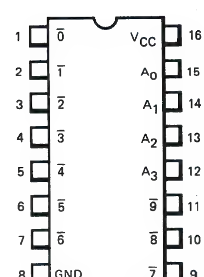
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the device ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the device is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS42XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS42XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	12	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		11 18	18 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		12 19	20 27	ns	Fig. 1	

AC WAVEFORMS

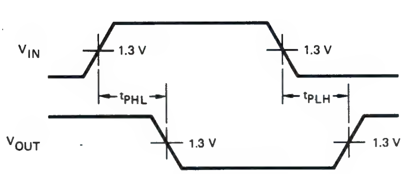


Fig. 1

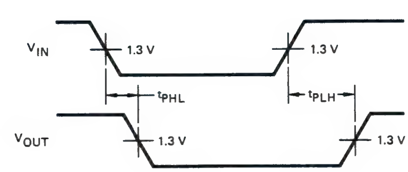


Fig. 2

F54LS/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

DESCRIPTION—The 54LS/74LS47 is Low Power Schottky BCD to 7-Segment Decoder/ Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

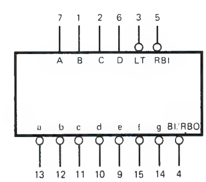
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the 54LS/74LS47 is designed to withstand the relatively high voltages required for 7-segment indicators.

The 54LS/74LS47 outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 24 mA of current may be driven directly from the 74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The 54LS/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) may be performed at any time which the $\overline{BI/BRO}$ node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

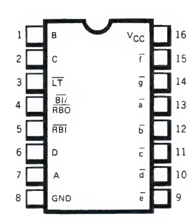
- **LAMP INTENSITY MODULATION CAPABILITY**
- **OPEN COLLECTOR OUTPUTS**
- **LAMP TEST PROVISION**
- **LEADING/TRAILING ZERO SUPPRESSION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **INPUTS FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

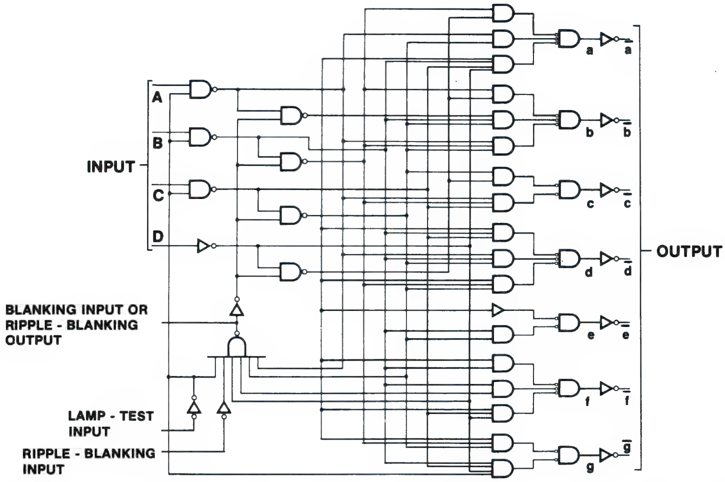


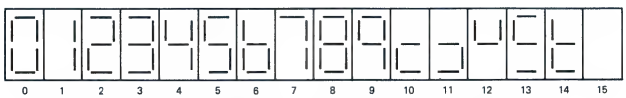
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple Blanking Output	1.2 U.L.	2.0 U.L.
$\bar{a}$, to $\bar{g}$	Outputs	Open Collector	15 (7.5) U.L.

Notes:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 7.5 U.L. for Military (XM) and 15 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS $\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}/\overline{RBO}$	OUTPUTS $\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS47XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS47XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM XC			0.7 0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage BI/RBO	XM,XC		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = MIN, V_{IN} = V_{IN}, or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 3.2 mA	
$I_{O\,(off)}$	Off State Output Current a thru g				2.5	V	V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table, $V_{O\,(off)}$ = 15 V	
$V_{O\,(on)}$	On State Outout Voltage a thru g	XM, XC		0.25	0.4	V	$I_{O\,(on)}$ = 12 mA	V_{CL} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	$I_{O\,(on)}$ = 24 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current BI/RBO Any Input except BI/RBO				1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			7	13	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment output			100 100	ns ns	$V_{CC} = 5.0$ V
t_{PHL} t_{PLH}	Propagation Delay, RBI Input To Segment Output			100 100	ns ns	$C_L = 15$ pF, $R_L = 665\Omega$

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are a $V_{CC} = 5.0$ V, $T_A = 25°C$.

AC WAVEFORMS

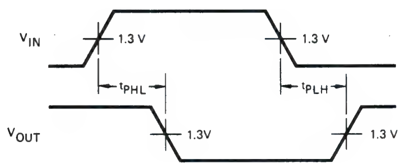


Fig. 1

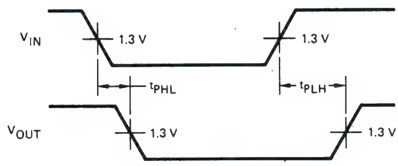


Fig. 2

5

F54LS/74LS48 • F54LS/74LS49
BCD TO 7-SEGMENT DECODER

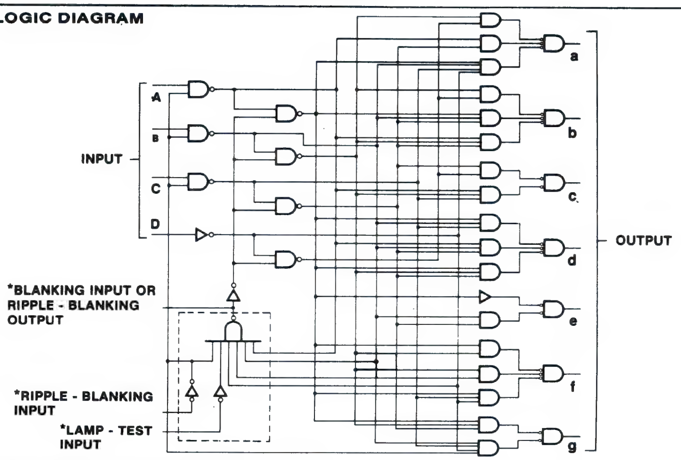
DESCRIPTION – The 54LS/74LS48 and 54LS/74LS49 are BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The 54LS/74LS49 offers active HIGH open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the 54LS/74LS48. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the 54LS/74LS49.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

The 54LS/74LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp Test ($\overline{LT}$) may be activated any time when the $\overline{BI}/\overline{RBO}$ node is HIGH. Both devices contain on overriding blanking input ($\overline{BI}$) which can be used to control the lamp intensity or to inhibit the outputs.

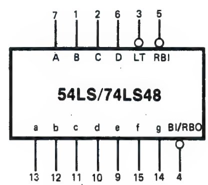
- **LAMP INTENSITY MODULATION CAPABILITY**
- **INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS ON 54LS/74LS48**
- **OPEN COLLECTOR OUTPUTS ON 54LS/74LS49**
- **INPUT CLAMP DIODES ELIMINATE HIGH-SPEED TERMINATION EFFECTS**
- **INPUTS FULLY TTL AND CMOS COMPATIBLE**

LOGIC DIAGRAM

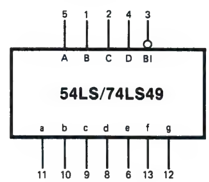


*Not included with the 54LS/74LS49

LOGIC SYMBOL

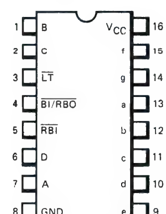


V_{CC} = Pin 16
GND = Pin 8

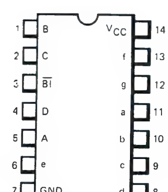


V_{CC} = Pin 14
GND = Pin 7

DIP (TOP VIEW)
54LS/74LS48



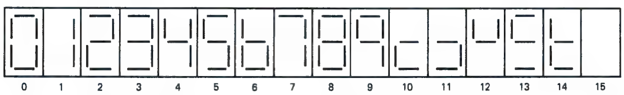
54LS/74LS49



PIN NAMES

		LOADING (Note a) HIGH	LOW
		0.5 U.L.	0.25 U.L.
A, B, C, D,	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{\text{RBI}}$	Ripple Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
$\overline{\text{LT}}$	Lamp Test (Active Low) Input	0.5 U.L.	0.75 U.L.
$\overline{\text{BI/RBO}}$	Blanking Input or Ripple	1.2 U.L.	2.0 U.L.
	Blanking Output (Active Low)	0.5 U.L.	0.25 U.L.
$\overline{\text{BI}}$	Blanking (Active Low) Input	Open Collector	3.75 (1.25) U.L. (48)
a to g	Outputs (Note b)	Open Collector	5 (2.5) U.L. (49)

NOTES:
a) Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 54LS/74LS48: 1.25 U.L. for Military (XM), 3.75 U.L. for Commercial (XC),
54LS/74LS49: 2.5 U.L. for Military (XM), 5 U.L. for Commercial (XC) Temperature Ranges.



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE
54LS/74LS48

DECIMAL OR FUNCTION	INPUTS $\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A	$\overline{\text{BI/RBO}}$	OUTPUTS a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H.	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

(1) $\overline{\text{BI/RBO}}$ is wired-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out ($\overline{\text{BI}}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{\text{BI/RBO}}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

TRUTH TABLE
54LS/74LS49

DECIMAL OR FUNCTION	INPUTS D	C	B	A	$\overline{\text{BI}}$	OUTPUTS a	b	c	d	e	f	g	NOTE
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{\text{BI}}$	X	X	X	X	L	L	L	L	L	L	L	L	2

NOTES:

(1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.

(2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS48 54LS49	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS48 74LS49	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type: F for Flatpack, D for Ceramic Dip. P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

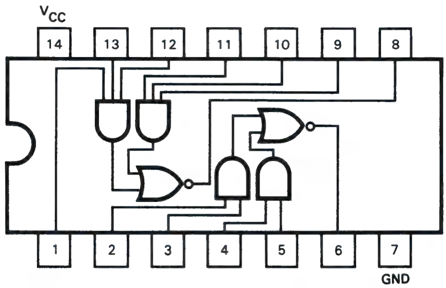
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guarantee Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XC			0.8	V	Guarantee Input LOW Voltage	
		XM			0.7	V		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_1 = −18 mA	
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{IH} = 2.0 V V_{IL} = V_{IL} MAX, V_{OH} = 5.5 V	
V_{OL}	Output LOW Voltage	XC, XM			0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IH} = 2.0 V
		XC			0.5	V	I_{OL} = 8 mA	V_{IL} = V_{IL} MAX
I_{IH}	Input Current HIGH				20 0.1	μA mA	V_{CC} = MAX, V_1 = 2.7 V V_{CC} = MAX, V_1 = 10 V	
I_{IL}	Input Current LOW				−0.4	mA	V_{CC} = MAX, V_1 = 0.4 V	
I_{CC}	Power Supply Current			8.0	15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from A input			100	ns	C_L = 15 pF, R_L = 2.0 kΩ, See Note 6
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from A input			100	ns	
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from $\overline{RBI}$ input			100	ns	C_L = 15 pF, R_L = 6.0 kΩ, See Note 6
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from $\overline{RBI}$ input			100	ns	

F54LS/74LS51

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS51XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS51XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.4	2.8	mA	V_{CC} = MAX, Inputs Open

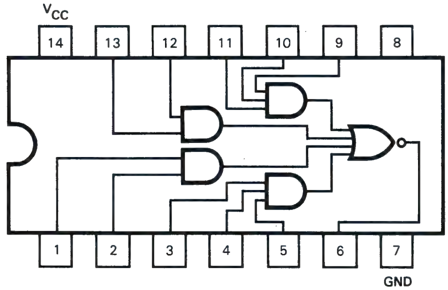
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS54

3-2-2-3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS54XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS54XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.0	2.0	mA	V_{CC} = MAX, Inputs Open

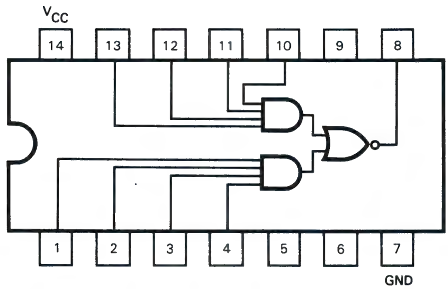
AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS55

2-WIDE 4-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS55XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS55XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.7	1.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

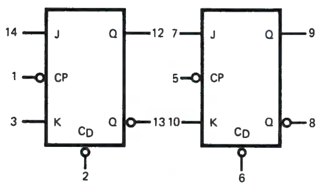
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS73

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

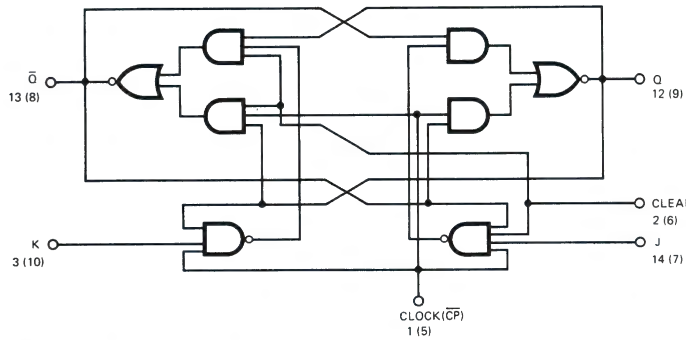
DESCRIPTION — The 54LS/74LS73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM
(Each Flip-Flop)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS73XM	4.5 V	5.0 V	5.5 V	−55° C to +125° C
74LS73XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Clear Clock				20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	J, K Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current J, K Clear Clock				−0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V	

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$t_WCP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_WCP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K TO Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

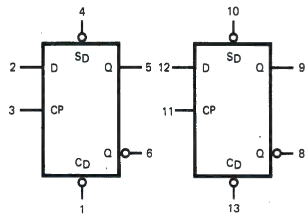
F54LS/74LS74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 54LS/74LS74 dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high-speed D-type flip-flops. Each flip-flop has individual Clear and Set inputs, and also complementary Q and $\overline{Q}$ Outputs.

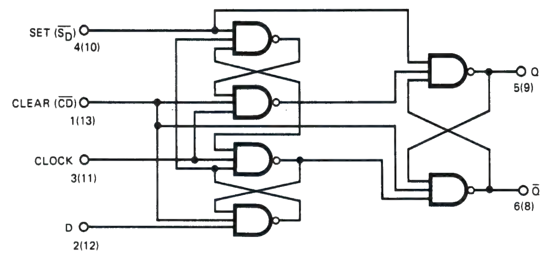
Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM (EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS74XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS74XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current Data Clock, Set Clear				 20 40 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Data Clock, Set Clear				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current Data Clock, Set Clear				 −0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	
t_{PLH}	Propagation Delay,			10	15	ns	Fig. 2	
t_{PHL}	Set or Clear to Output	CP = L		18	24			
t_{PHL}		CP = H		26	35			

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	$V_{CC} = 5.0$ V
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	10	6		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−14		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	14		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−6		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°$C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

F54LS/74LS75 • F54LS/74LS77

4-BIT D LATCH

DESCRIPTION—The TTL/MSI 54LS/74LS75 and 54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The 54LS/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the 54LS/74LS77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}$–$\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 Unit Load (U.L.) = 40μA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

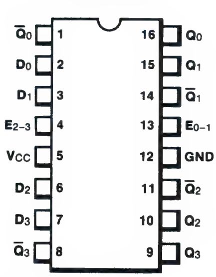
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

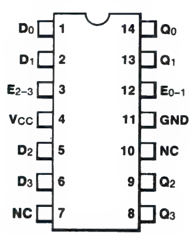
NOTES:
t_n = bit time before clock negative-going transition
t_{n+1} = bit time after clock negative-going transition.

CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/75LS75

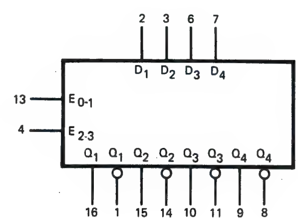


54LS/74LS77



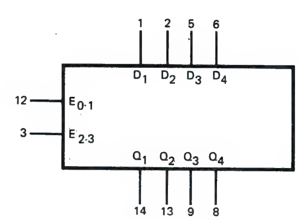
LOGIC SYMBOLS

F54LS/74LS75



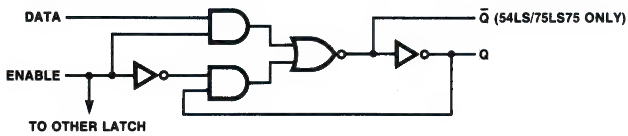
V_{cc} = Pin 5
GND = Pin 12

F54LS/74LS77



V_{cc} = Pin 4
GND = Pin 11
NC = Pin 7, 10

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential-to-Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS75XM 54LS77XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS75XC 74LS77XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; D for Flatpak, P for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM XC			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM XC	2.5 2.7	3.4 3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM, XC XC		0.25 0.35	0.4 0.5	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} I_{OL} = 8.0 mA or V_{IL} per Truth Table
I_{IH}	Input HIGH Current D E				20 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage D E				0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current D E				−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Note more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

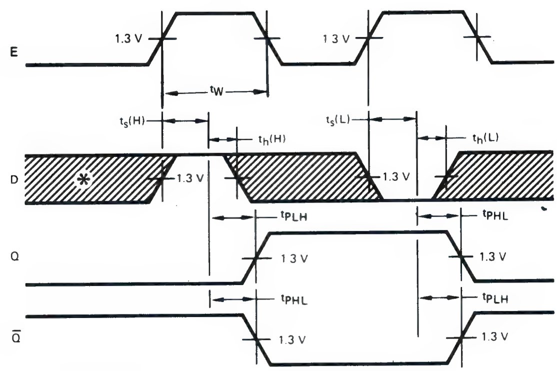
SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, D to Q			27 17	ns	V_{CC} = 5.0 V C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, D to $\overline{Q}$ (LS75)			20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q			27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay			30 15	ns	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wCP	Minimum Enable Pulse Width	20			ns	Fig. 1
t_s	Set-up Time, Data to Enable (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Enable (HIGH or LOW)	0			ns	Fig. 1

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$, and maximum loading.
5. Not more than one output should be shorted at a time.

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

5

F54LS/74LS76

DUAL JK FLIP-FLOP WITH SET AND CLEAR

DESCRIPTION — The 54LS/74LS76 offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

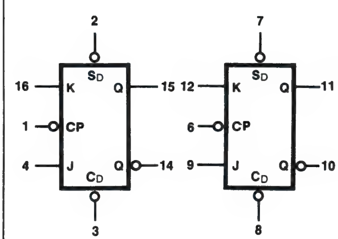
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

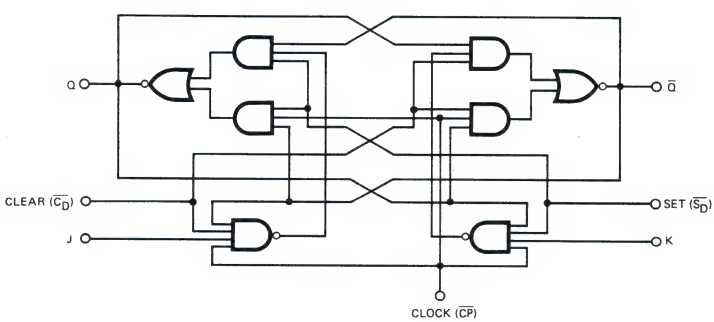
H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Immaterial
l,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS76XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS76XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current J, K Set, Clear Clock				 20 60 80	μA	V_{CC} = MAX, V_{In} = 2.7 V	
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current J, K Set, Clear Clock				 −0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V	

AC CHARACTERISTICS: T_A = 25°C (See Page for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		16 16	 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See Page for Waveforms

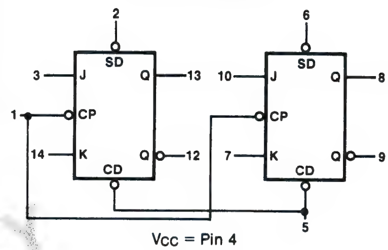
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_wCP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
$t_wCP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

F54LS/74LS78
DUAL JK FLIP FLOP

DESCRIPTION — The 54LS/74LS78 offers individual J, K, and Direct Set inputs as well as common Clock Pulse and Common Direct Clear Inputs. These dual Flip-Flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW Clock Transition.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS78XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS78XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current J, K Set, Clear Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current J, K Set, Clear Clock				 −0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V	

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$t_WCP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_WCP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°$C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

F54LS/74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

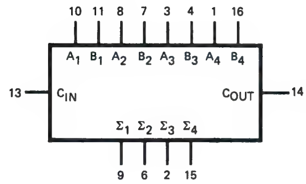
DESCRIPTION—The 54LS/74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 — A_4, B_1 — B_4) and a Carry Input (C_{IN}). It generates the binary Sum outputs (Σ_1 — Σ_4) and the Carry Output (C_{OUT}) from the most significant bit. It operates with either HIGH or active LOW operands (positive or negative logic.) The 54LS/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

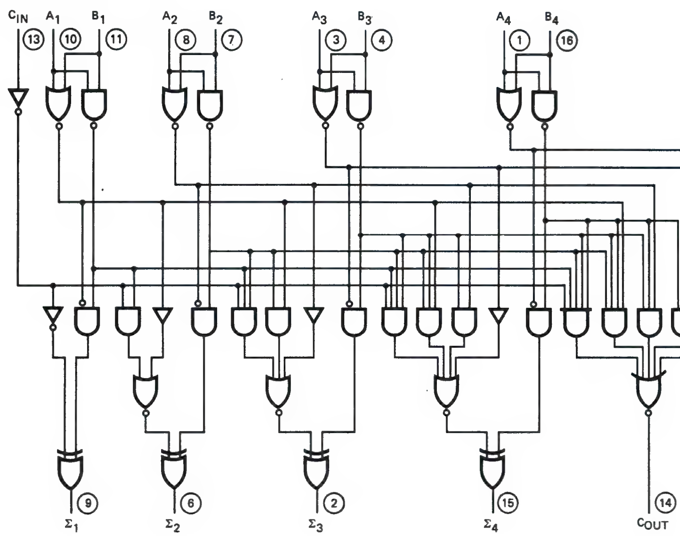
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



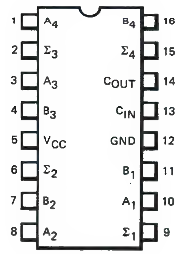
V_{CC} = Pin 5
GND = Pin 12

LOGIC DIAGRAM



V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION—This device adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the device can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS83AXM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS83AXC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output		14 13	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		17 19	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to $\overline{C_{OUT}}$ Output		12 9	17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output		14 10	17 17	ns	

AC WAVEFORMS

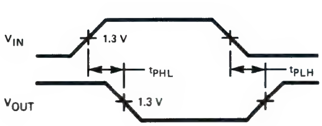


Fig. 1

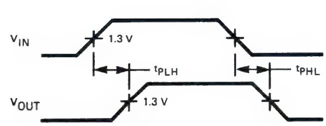


Fig. 2

F54LS/74LS85

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION — The 54LS/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the 54LS/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

PIN NAMES

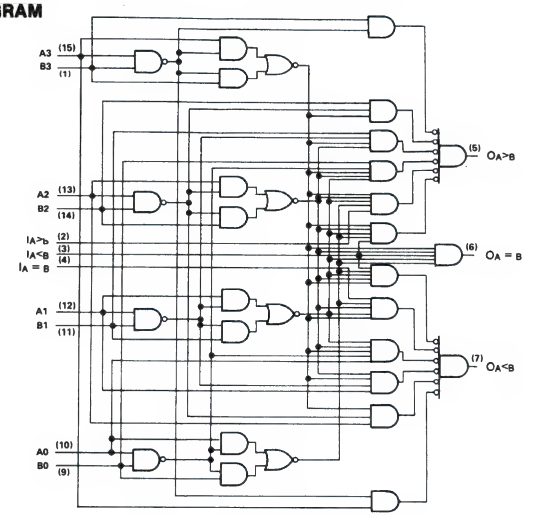
PIN NAMES		LOADING (Note a) HIGH	LOW
A_0-A_3, B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

Notes:

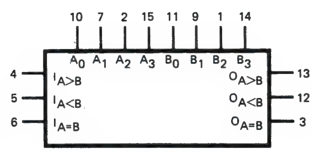
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6mA LOW

b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM

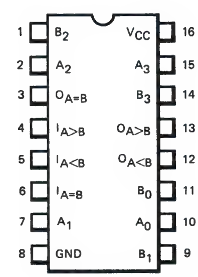


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

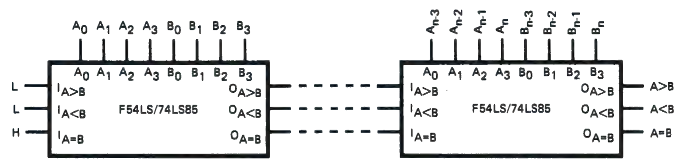
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS85XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS85XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.



L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

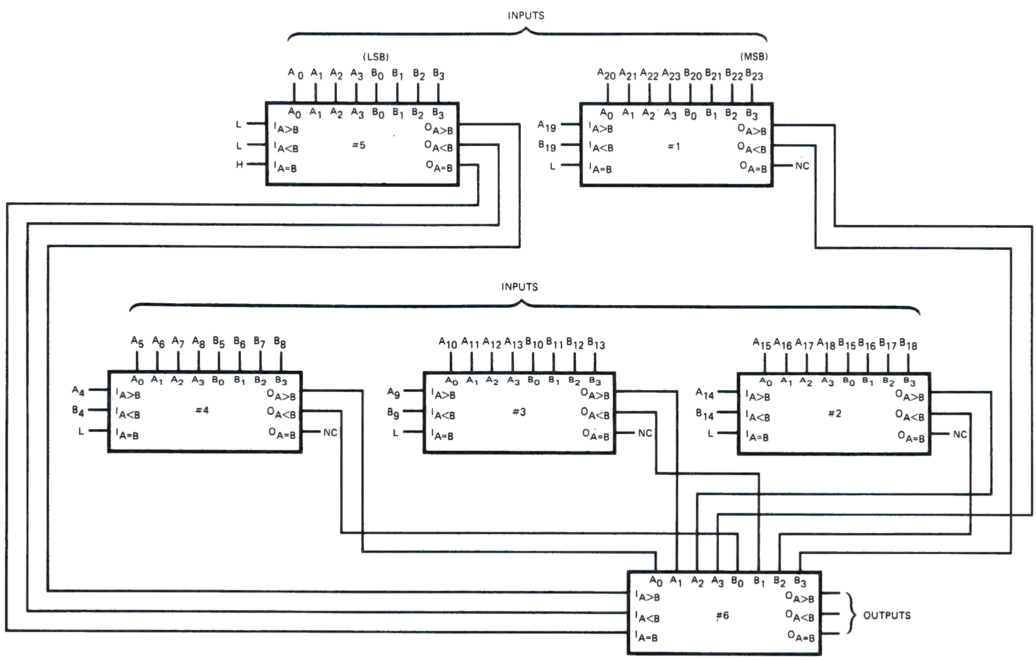
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The 54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.5		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.5			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current A_0-A_3, B_0-B_3, $I_{A=B}$ $I_{A<B}$, $I_{A>B}$				60 20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	A_0-A_3, B_0-B_3, $I_{A=B}$ $I_{A<B}$, $I_{A>B}$				0.3 0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current A_0-A_3, B_0-B_3, $I_{A=B}$ $I_{A<B}$, $I_{A>B}$				−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			11	20	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operaing ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Any A or B Data Input to Any Output		25 20	36 30	ns	Fig. 1, 2
t_{PLH} t_{PHL}	$I_{A=B}$ Input to $O_{A>B}$ or $O_{A<B}$ Output		15 12	22 17	ns	Fig. 1, 2
t_{PLH} t_{PHL}	$I_{A=B}$ Input to $O_{A=B}$ Output		14 12	12 17	ns	Fig. 1, 2
t_{PLH} t_{PHL}	$I_{A>B}$ or $I_{A<B}$ Input to Any Output		25 20	36 30	ns	Fig. 1, 2

AC WAVEFORMS

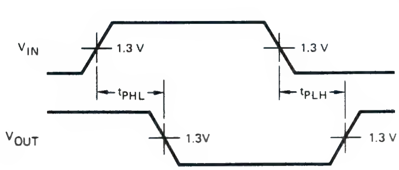


Fig. 1

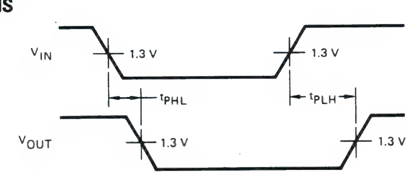
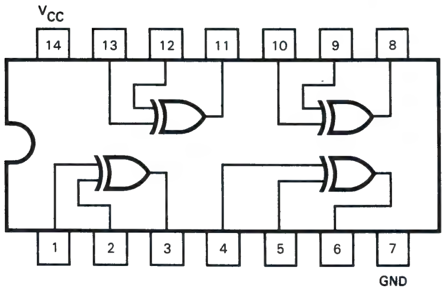


Fig. 2

F54LS/74LS86

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS86XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS86XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

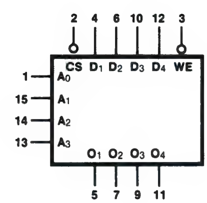
F54LS/74LS89

64-BIT RANDOM ACCESS MEMORY WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION—The 54LS/74LS89 is a high-speed, low-power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) are HIGH. For all other combinations of $\overline{CS}$ and $\overline{WE}$ the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

AN	Address Input
$\overline{CS}$	Chip Select (active LOW) Input
D_n	Data Input
$\overline{O_n}$	Data (inverted) Output
$\overline{WE}$	Write Enable (active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	H	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Entry	Complement of Data Inputs
H	H	Hold	HIGH (Off)

H = HIGH Voltage Level
L = LOW Voltage Level

F54LS/74LS90 • F54LS/74LS92

DECADE COUNTER DIVIDE-BY-TWELVE COUNTER

F54LS/74LS93

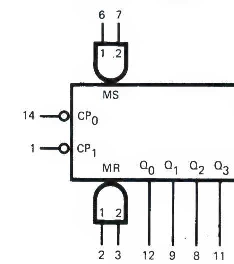
4-BIT BINARY COUNTER

DESCRIPTION—The 54LS/74LS90, 54LS/74LS92 and 54LS/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (54LS/74LS90), divide-by-six (54LS/74LS92) or divide-by-eight (54LS/74LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the 54LS/74LS90 also has a 2-input gated Master Set (Preset 9).

- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH-COUNT RATES . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

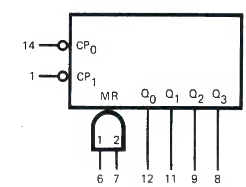
LOGIC SYMBOL

54LS/74LS90



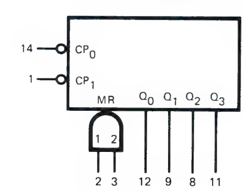
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

54LS/74LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

54LS/74LS93



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

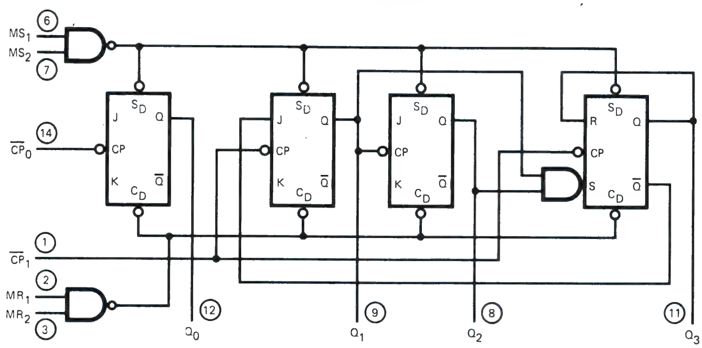
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (54LS/74LS90, ÷6 Section (54LS/74LS92)	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (54LS/74LS93)	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, 54LS/74LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (54LS/74LS90), ÷6 (54LS/74LS92), ÷8 (54LS/74LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.

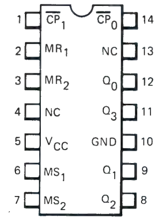
LOGIC DIAGRAM

54LS/74LS90



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

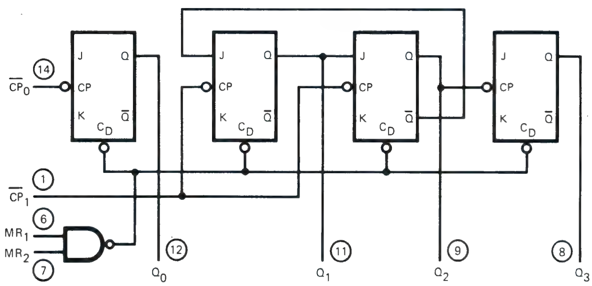


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

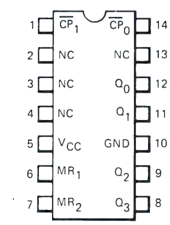
LOGIC DIAGRAM

54LS/74LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

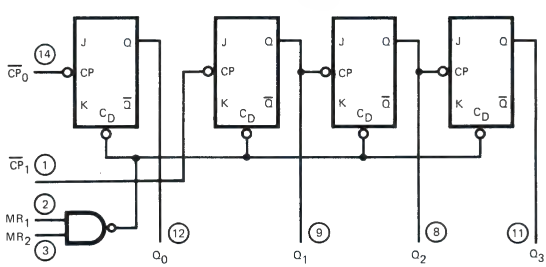


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

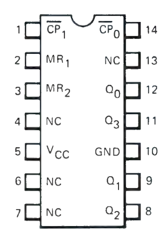
LOGIC DIAGRAM

54LS/74LS93



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION—These devices are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (54LS/74LS90), divide-by-six (54LS/74LS92), or divide-by-eight (54LS/74LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the 54LS/74LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

54LS/74LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

54LS/74LS92

A. Modulo-12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operations at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

54LS/74LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through center.

54LS/74LS90 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

54LS/74LS92 AND 54LS/74LS93 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

54LS/74LS90 BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

54LS/74LS92 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input CP_1.

54LS/74LS93 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS90XM 54LS92XM 54LS93XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS90XC 74LS92XC 74LS93XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				 20 120 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	MS, MR $\overline{CP}_0$, $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				0.1 0.4 0.8	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				 −0.4 −2.4 −1.6 −3.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		MHz	Fig. 1
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		MHz	Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	ns	Fig. 1
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	ns	
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30					ns	Fig. 3
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		40					ns	Fig. 2
t_{PHL}	MR Input to Any Output		40		40		40	ns	Fig. 2

AC SET-UP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns	Fig. 1
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns	
t_W	MS Pulse Width	15						ns	Fig. 2, 3
t_W	MR Pulse Width	15		15		15		ns	Fig. 2
t_{rec}	Recovery Time MS to $\overline{CP}$	25						ns	Fig. 2, 3
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns	Fig. 2

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

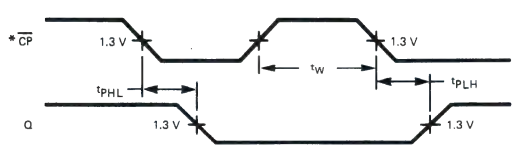


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

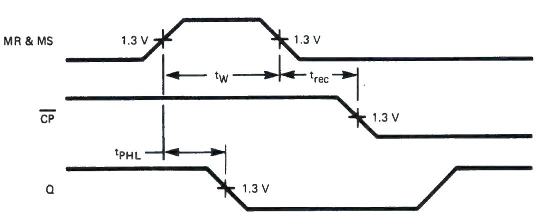


Fig. 2

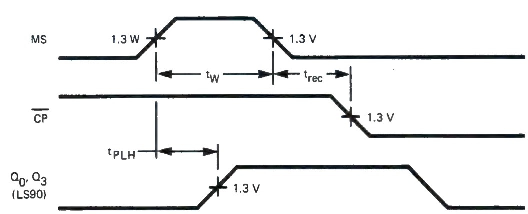


Fig. 3

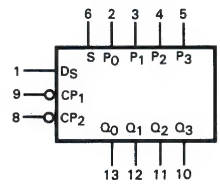
F54LS/74LS95B
4-BIT SHIFT REGISTER

DESCRIPTION—The 54LS/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SYNCHRONOUS, EXPANDABLE SHIFT RIGHT**
- **SYNCHRONOUS SHIFT LEFT CAPABILITY**
- **SYNCHRONOUS PARALLEL LOAD**
- **SEPARATE SHIFT AND LOAD CLOCK INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



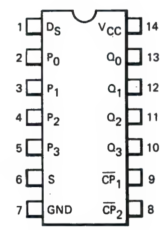
V_{CC} = Pin 14
GND = Pin 7

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

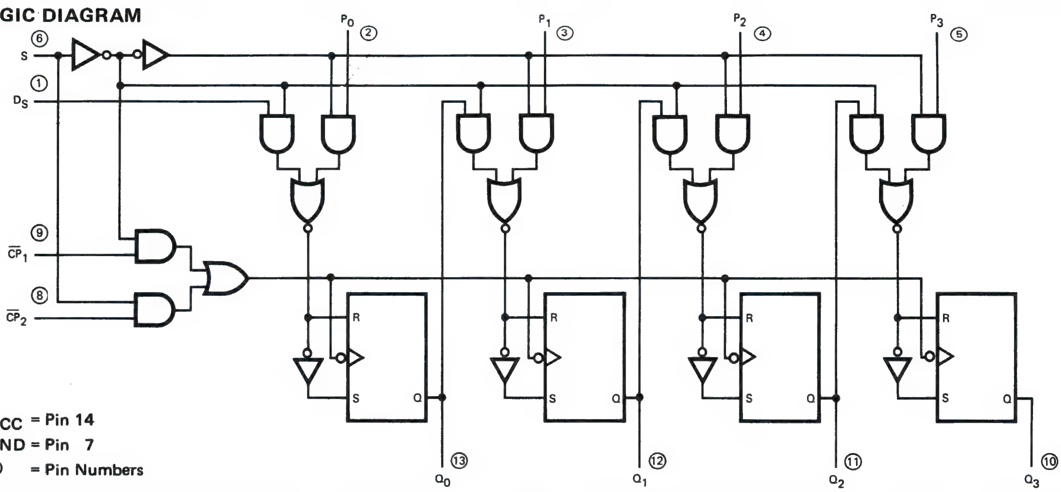
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION—This device is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 — P_3) Data inputs and four Parallel Data outputs (Q_0 — Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the P_0 — P_3 inputs to the Q_0 — Q_3 outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the device in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW-to-HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH-to-LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	↓	X	p_n	p_0	p_1	p_2	p_3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H	L	X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS95BXM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS95BXC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current S, D_S, P_0, P_1, P_2, P_3 $\overline{CP}_1$, $\overline{CP}_2$				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	S, D_S, P_0, P_1, P_2, P_3 $\overline{CP}_1$, $\overline{CP}_2$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current S, D_S, P_0, P_1, P_2, P_3 $\overline{CP}_1$, $\overline{CP}_2$				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 18	27 27	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	20			ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	10			ns		
t_{sL}	Set-up Time, LOW Mode Control to Clock	20			ns	Fig. 2	
t_{hL}	Hold Time, LOW Mode Control to Clock	0			ns		
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			ns	Fig. 2	
t_{hH}	Hold Time, HIGH Mode Control to Clock	0			ns		

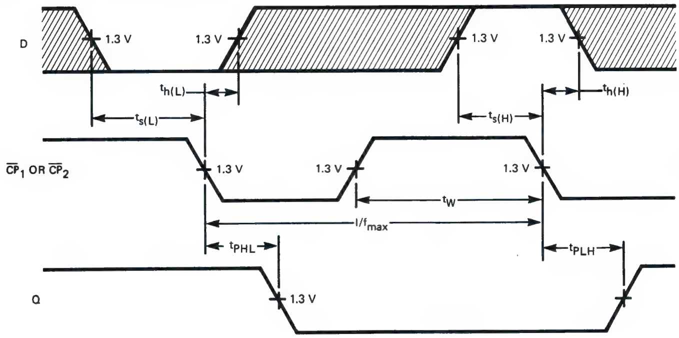
DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is (D_S for $\overline{CP_1}$) or (P_n for $\overline{CP_2}$).

Fig. 1

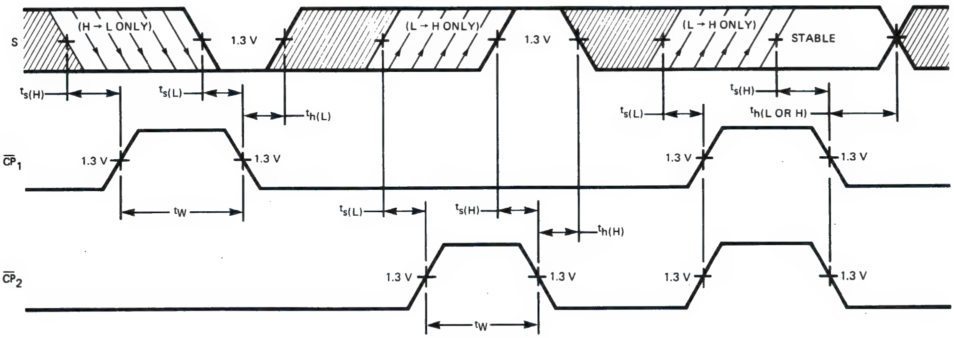


Fig. 2

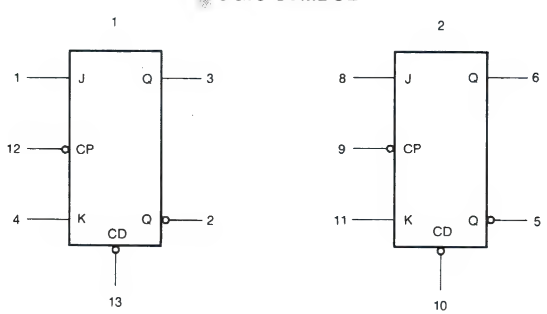
F54LS/74LS107

DUAL JK FLIP-FLOP

DESCRIPTION — the 54LS/74LS107 is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

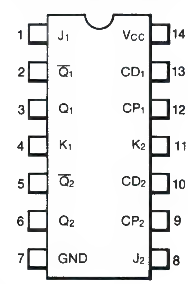
The 54LS/74LS107 is the same as the 54LS/74LS73, but has corner power pins. For electrical characteristics, truth tables and operations information, refer to the 54LS/74LS73 data sheet.

LOGIC SYMBOL



V_{CC} = 14
GND = 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS107XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS107XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

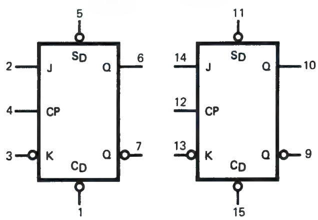
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

F54LS/74LS109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

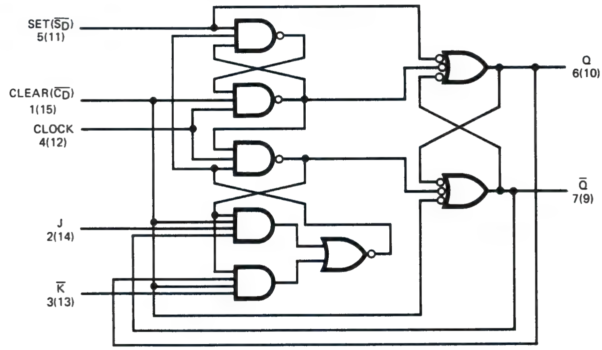
DESCRIPTION—The 54LS/74LS109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together. The 54LS/74LS109 is a pin-for-pin replacement of the 9024 and 9L24.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS109XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS109XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Clock, Set Clear				 20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Clock, Set Clear				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Clock, Set Clear				 −0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	
t_{PLH}	Propagation Delay, Set or Clear to Output			10	15	ns	Fig. 2	
t_{PHL}		CP = L		18	24			
t_{PHL}		CP = H		26	35			

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_W CP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, Data to Clock	18	12		ns	Fig. 1	
$t_h(H)$	Hold Time HIGH, Data to Clock	0	−13		ns		
$t_s(L)$	Set-up Time LOW, Data to Clock	20	13		ns		
$t_h(L)$	Hold Time LOW, Data to Clock	0	−12		ns		

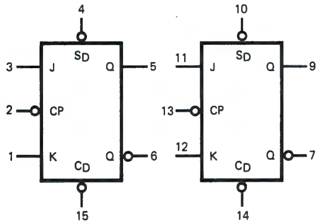
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°$ C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

F54LS/74LS112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

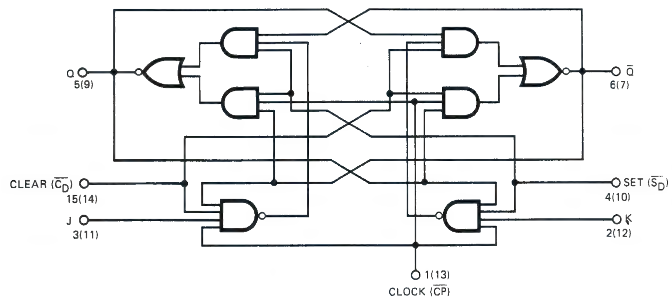
DESCRIPTION—The 54LS/74LS112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as a minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS112XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS112XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Set, Clear Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set, Clear Clock				 −0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_W CP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_W CP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

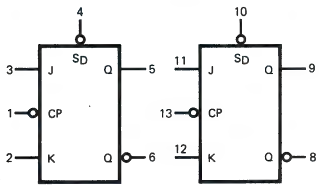
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°$C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

F54LS/74LS113

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

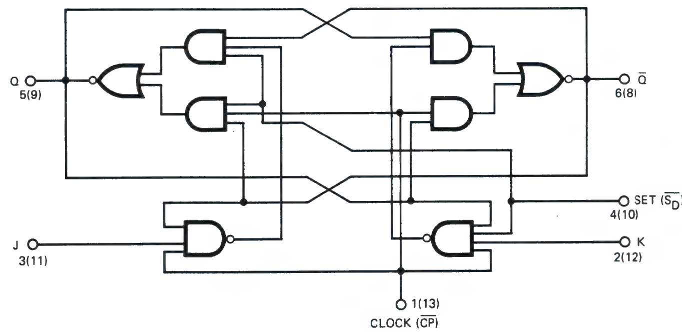
DESCRIPTION—The 54LS/74LS113 offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS113XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS113XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Set Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clock				 −0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

5

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_WCP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_WCP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

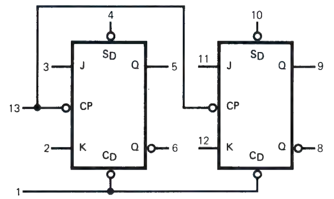
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

F54LS/74LS114

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

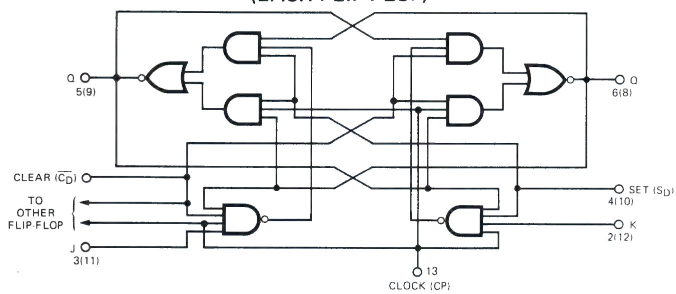
DESCRIPTION—The 54LS/74LS114 offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS114XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS114XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Set Clear Clock				 20 60 120 160	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clear Clock				0.1 0.3 0.6 0.8	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clear Clock				 −0.36 −0.8 −1.6 −1.44	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

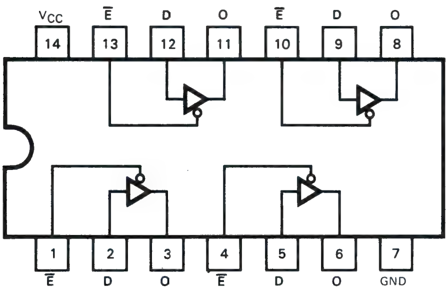
AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

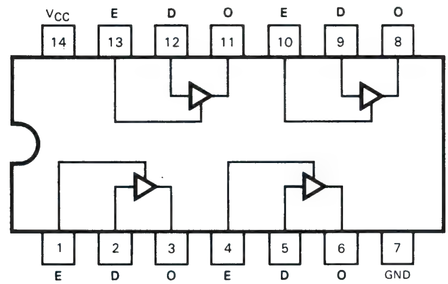
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_W CP(H)$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_W CP(L)$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns		
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

F54LS/74LS125 • F54LS/74LS126

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES





5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
54LS125XM 54LS126XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS125XC 74LS126XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW	54LS/74LS125			16	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\bar{E}}$ = 0 V	
		54LS/74LS126			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
	Power Supply Current, Outputs Off	54LS/74LS125			20	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\bar{E}}$ = 4.5 V	
		54LS/74LS126			24	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 0 V	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRUTH TABLES

54LS/74LS125

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

54LS/74LS126

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
(Z) = High Impedance (off)

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS125 MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			15 18	ns	Fig. 2	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667$
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	
t_{PZL}	Output Enable Time to LOW Level			25	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level			20	ns	Figs. 3, 5	$V_{CC} = 5.0$ V $C_L = 5$ pF $R_L = 667$
t_{PHZ}	Output Disable Time from HIGH Level			20	ns	Figs. 4, 5	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS126 MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			15 18	ns	Fig. 2	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667$
t_{PZH}	Output Enable Time to HIGH Level			20	ns	Figs. 4, 5	
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	$V_{CC} = 5.0$ V $C_L = 5$ pF $R_L = 667$
t_{PHZ}	Output Disable Time from HIGH Level			25	ns	Figs. 4, 5	

AC WAVEFORMS

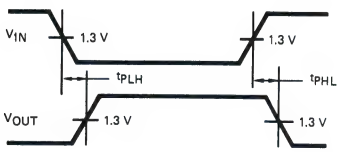


Fig. 1

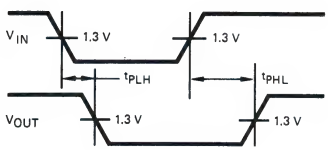


Fig. 2

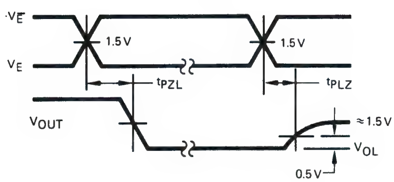


Fig. 3

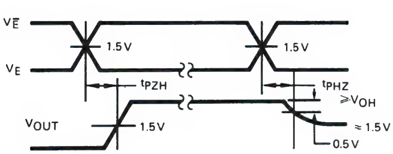
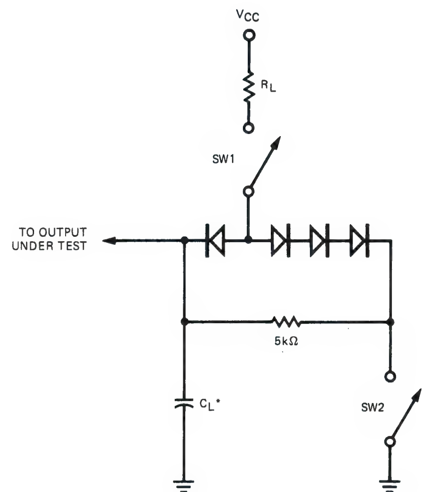


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

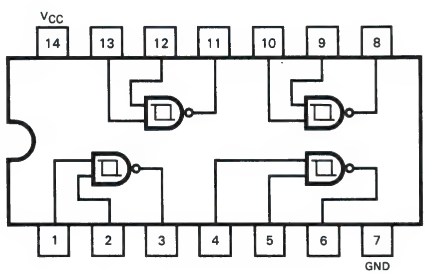
F54LS/74LS132

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

DESCRIPTION—The54LS/74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+}(MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

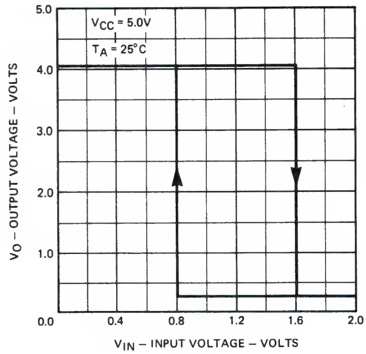


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
POWER SUPPLY VOLTAGE

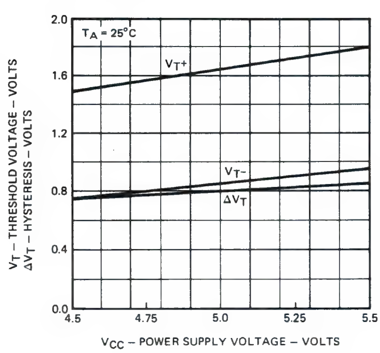


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
TEMPERATURE

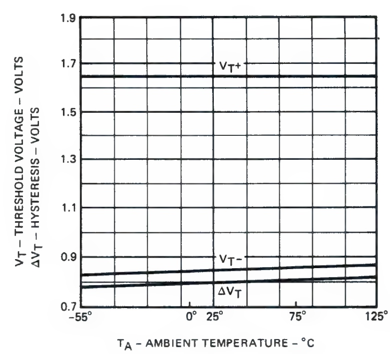


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS132XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS132XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

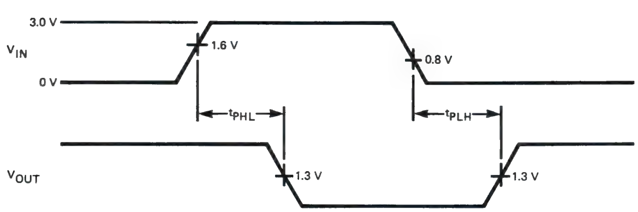
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage			1.6		V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage			0.8		V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			5.9	11	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.2	14	mA	V_{CC} = MAX, V_{IN} = 4.5 V

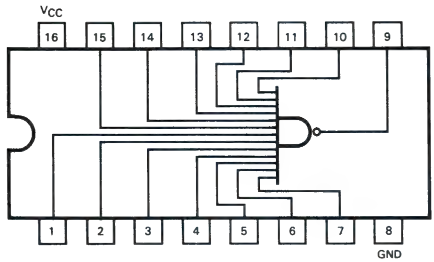
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



F54LS/74LS133
13-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS133XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS133XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

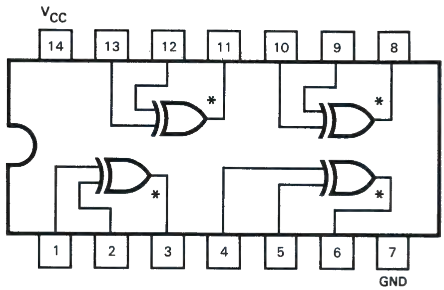
AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		25	38	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS136

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

*Open Collector Outputs

5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS136XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS136XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

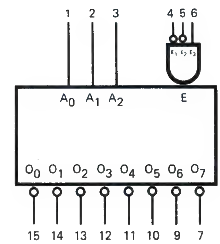
F54LS/74LS138

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION—The 54LS/74LS138 is a MSI high-speed 1-of-8 Decoder/Demultiplexer. It is ideally suited for high bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three devices or to a 1-of-32 decoder using four devices and one inverter. It is fabricated with the Schottky barrier diode process for high-speed and is completely compatible with all Fairchild TTL families.

- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **TYPICAL POWER DISSIPATION OF 32 mW**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



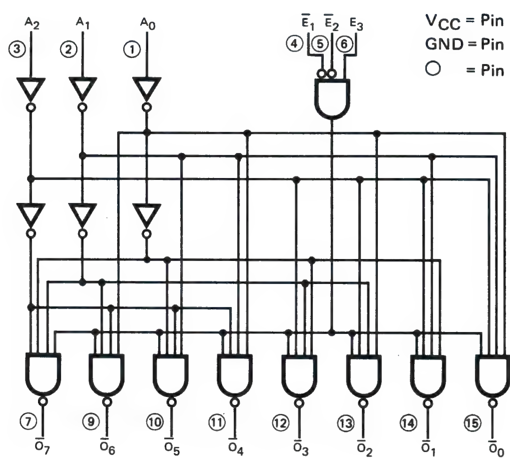
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

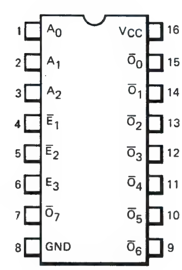
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION—This device is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). It features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four devices and one inverter. (See Figure a.)

The device can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

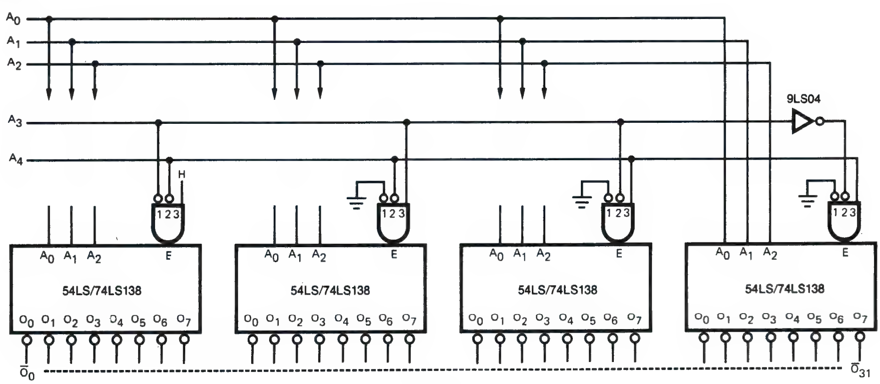


Fig. a.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS138XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS138XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_1$ or $\overline{E}_2$ to Output		9.0 17	15 24	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, E_3 to Output		11 20	18 28	ns	Fig. 1	

AC WAVEFORMS

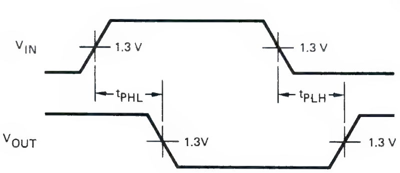


Fig. 1

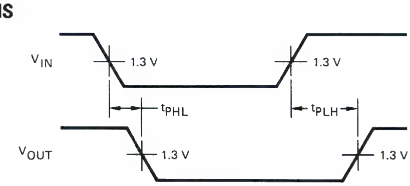


Fig. 2

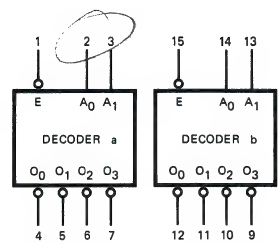
F54LS/74LS139

DUAL 1-OF-4 DECODER

DESCRIPTION—The 54LS/74LS139 is a MSI high-speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the device can be used as a function generator providing all four minterms of two variables. It is fabricated with the Schottky barrier diode process for high-speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



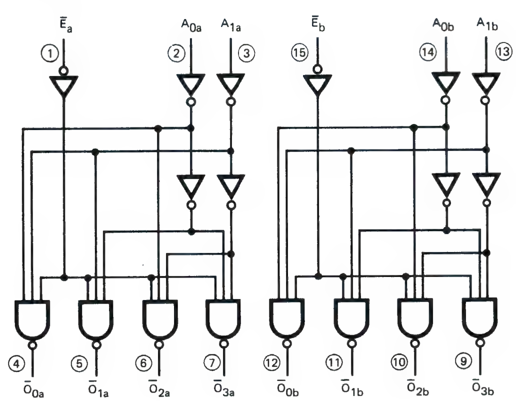
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

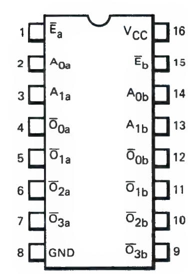
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — This device is a high-speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the device generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

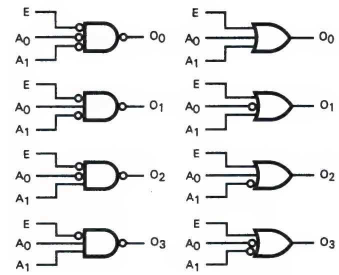


Fig. a

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS139XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS139XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.8	11	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		9.0 17	15 24	ns	Fig. 2	

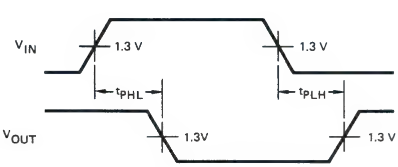


Fig. 1

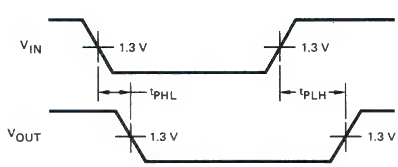


Fig. 2

5

F54LS/74LS145
1-OF-10 DECODER/DRIVER

DESCRIPTION—The 54LS/74LS145, 1-of-10 Decoder/Driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families.

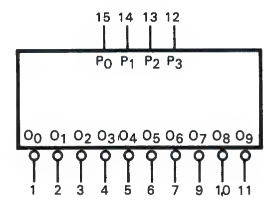
- **LOW POWER VERSION OF 54/74145**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

LOADING (Note a)

PIN NAMES		HIGH	LOW
P_0, P_1, P_2, P_3	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs (Note b)	Open Collector	15 (7.5) U.L.

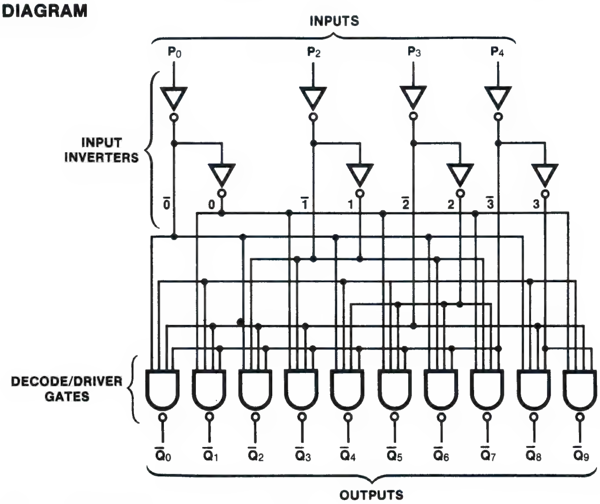
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges

LOGIC SYMBOL

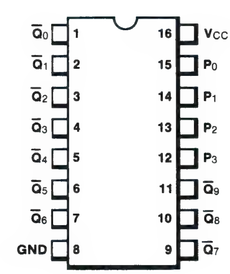


V_{CC} = 16
GND = 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

INPUTS				OUTPUTS									
P_D	P_C	P_B	P_A	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS145XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS145XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL} or V_{IH} per Truth Table	
		XC	2.7	3.5				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short-Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			7	13	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PHL} t_{PLH}	Propagation Delay P_n Input to Q_n Output			50 50	ns	Figs. 1, 2	V_{CC} = 5.0 V C_L = 15 pF

AC WAVEFORMS

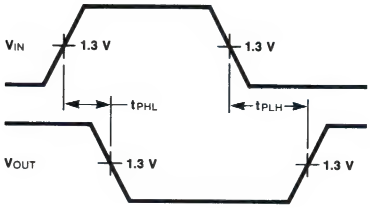


Fig.1

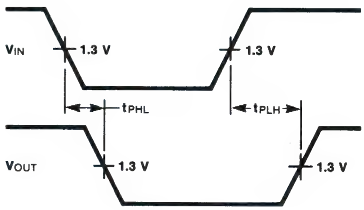


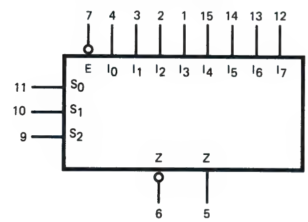
Fig. 2

F54LS/74LS151
8-INPUT MULTIPLEXER

DESCRIPTION—The 54LS/74LS151 is a MSI high-speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It also can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

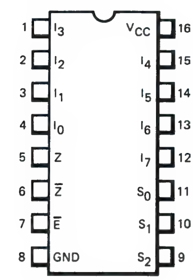
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



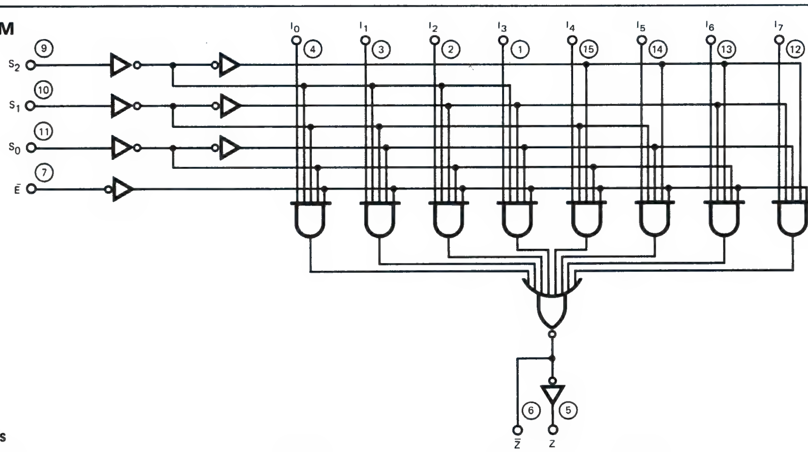
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 +$$
$$I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The device provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, it can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS151XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS151XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.0	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	41 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Z}$ Output		13 17	20 26	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Z Output		22 18	33 27	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	26 23	ns	Fig. 2	

AC WAVEFORMS

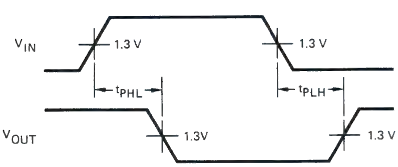


Fig. 1

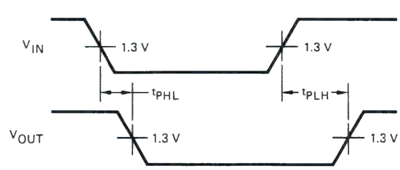


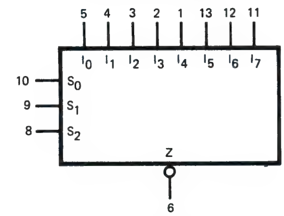
Fig. 2

F54LS152
8-INPUT MULTIPLEXER

DESCRIPTION — The 54LS152 is a MSI high-speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. It is supplied in FLATPAK only; for Dual In-line Package application use the 74LS151.

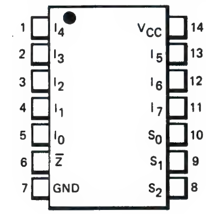
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
FLATPAK (TOP VIEW)



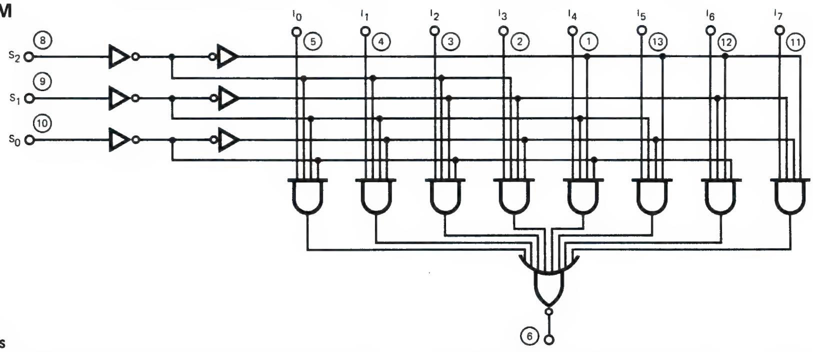
Dot Indicates Pin 1

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The logic function provided at the output is:

$$\overline{Z} = (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 +$$
$$I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

This device provides the ability, in one package, to select from eight sources of data or control information.

TRUTH TABLE

S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$
X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS152FM	4.5 V	5.0 V	5.5 V	−55°C to +125°C

See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			5.6	9.0	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		12 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		8.0 10	13 15	ns	Fig. 1	C_L = 15 pF

AC WAVEFORMS

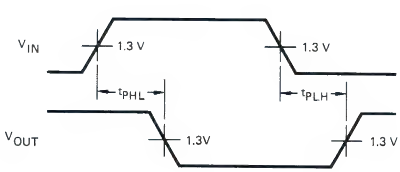


Fig. 1

F54LS/74LS153

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The 54LS/74LS153 is a MSI very high-speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the device can generate any two functions of three variables. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

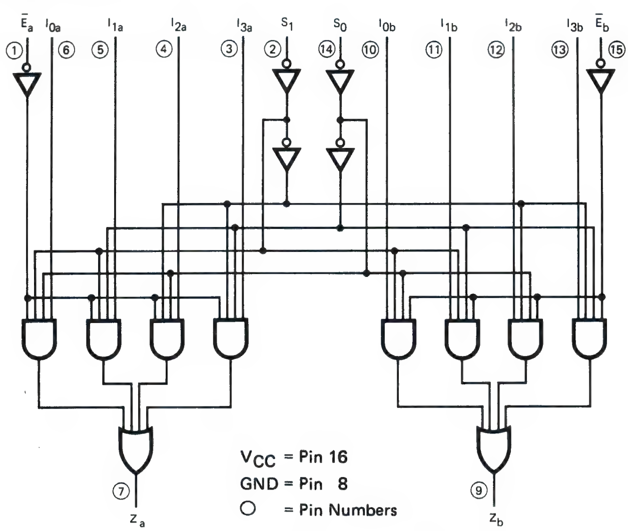
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **SEPARATE ENABLE FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1, I_2, I_3	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

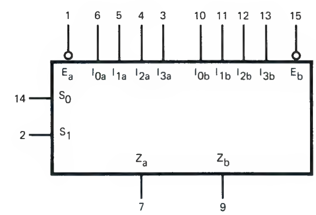
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



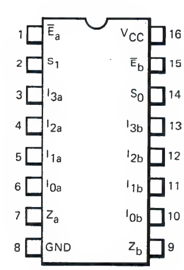
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — This device is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high-speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The device can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. It can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS153XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS153XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		20 16	29 24	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		17 14	24 20	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 2	

AC WAVEFORMS

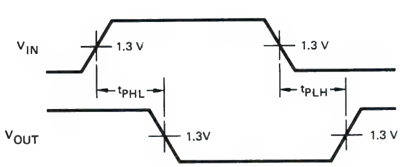


Fig. 1

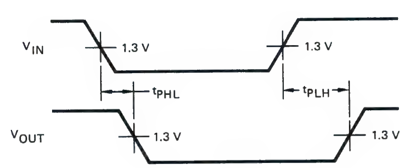


Fig. 2

F54LS/74LS155 • F54LS/74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER
(54LS/74LS156 HAS OPEN COLLECTOR OUTPUTS)

DESCRIPTION — The 54LS/74LS155 and 54LS/74LS156 are MSI high-speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The 54LS/74LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

These devices are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **COMMON ADDRESS INPUTS**
- **TRUE OR COMPLEMENT DATA DEMULTIPLEXING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

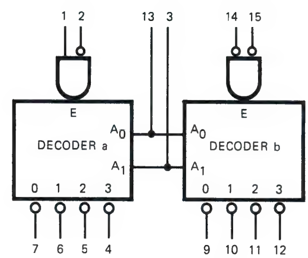
		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a$, $\overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

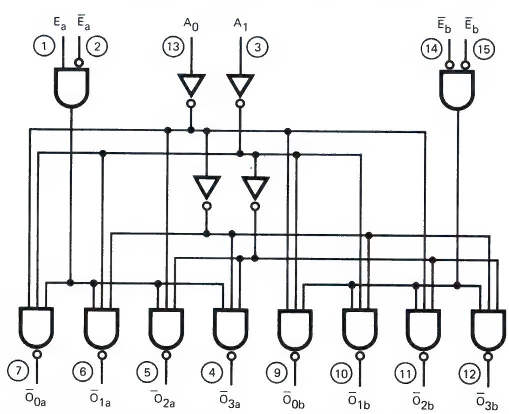
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The HIGH level drive for the 9LS156 must be established by an external resistor.

LOGIC SYMBOL



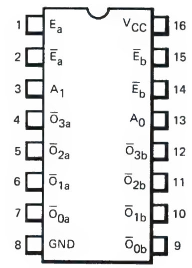
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — These devices are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$—$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($\overline{E}_a \cdot E_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). Either can be used as a 1-of-8 Decoder/Demultiplexer by trying E_a to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

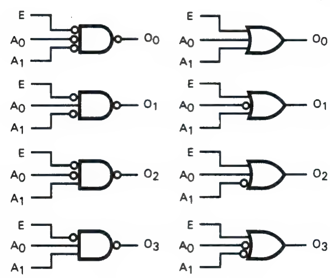
The devices can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The 54LS/74LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

where $E = E_a + \overline{E}_a$; $E = E_b + E_b$

15

15 14



6

Fig. a

A13 A12

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS155XM 54LS156XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS155XC 74LS156XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage 9LS155 Only	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
I_{OH}	Output HIGH Current 9LS156 Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		9LS155		9LS156				
		TYP	MAX	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	11 19	18 27	18 23	28 33	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	9.0 17	15 24	16 21	25 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	11 20	18 28	18 24	28 34	ns	Fig. 1	

AC WAVEFORMS

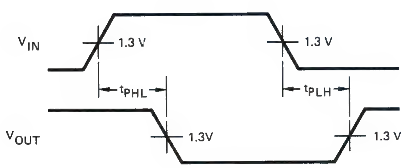


Fig. 1

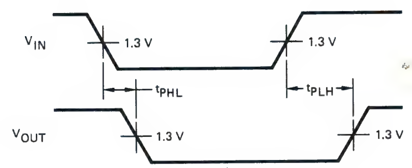


Fig. 2

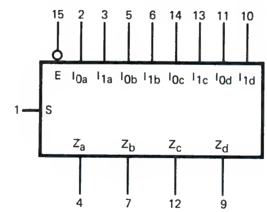
F54LS/74LS157

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The 54LS/74LS157 is a MSI high-speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. It can also be used to generate any four of the 16 different functions of two variables. The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



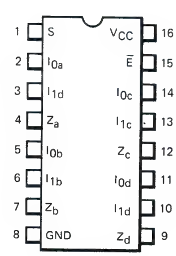
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

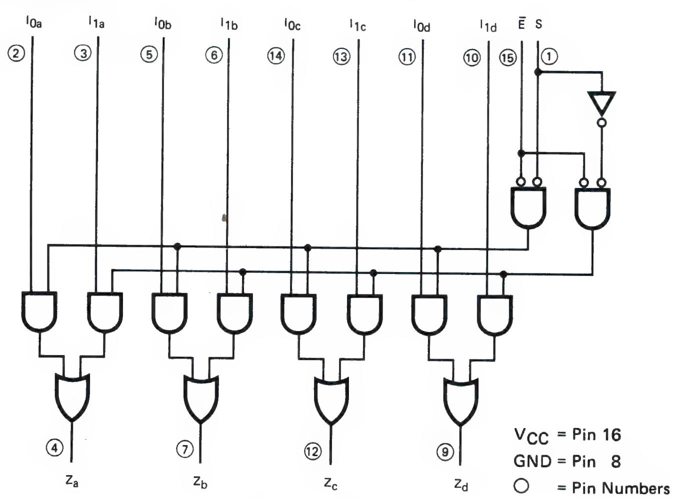
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of this device is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. It can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS157XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS157XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

F54LS/74LS165

8-BIT PARALLEL-TO-SERIAL CONVERTER

DESCRIPTION—The 54LS/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_1, CP_2	Clock (LOW-to-HIGH Going Edge) Inputs	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	1.5 U.L.	0.75 U.L.
P_0-P_7	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_7	Serial Output from Last State (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_7$	Complementary Output (Note b)	10 U.L.	5 (2.5) U.L.

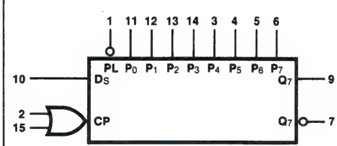
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

TRUTH TABLE

$\overline{PL}$	CP 1	CP 2	CONTENTS Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	$\overline{Q}_7$	RESPONSE
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↑	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↑	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↑	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↑	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

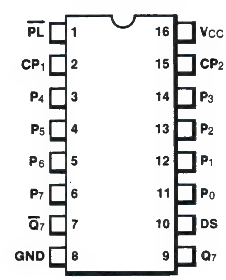
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL



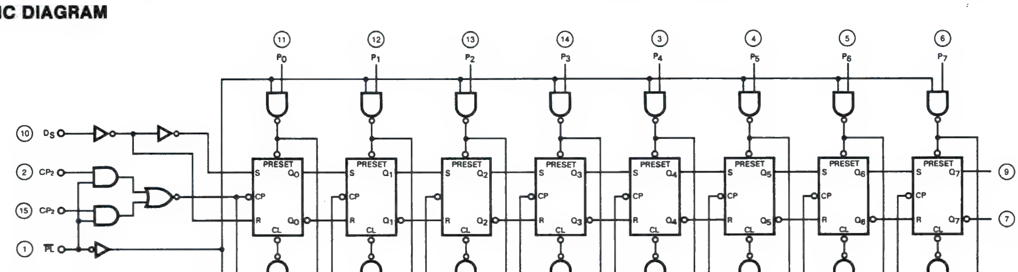
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○= Pin Number

F54LS/74LS158

QUAD 2-INPUT MULTIPLEXER

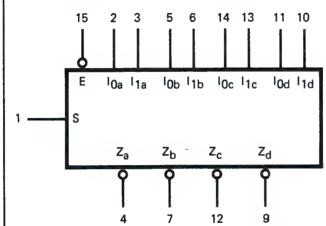
DESCRIPTION—The 54LS/74LS158 is a MSI high-speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The device can also generate any four of the 16 different functions of two variables. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INVERTED OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		**LOADING (Note a)**	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

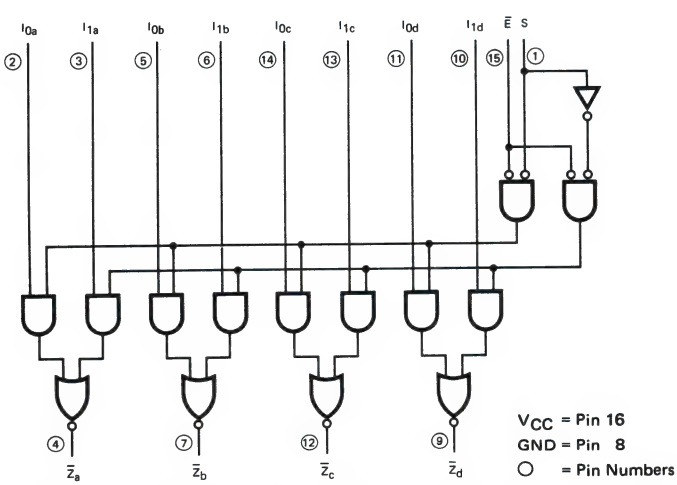
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



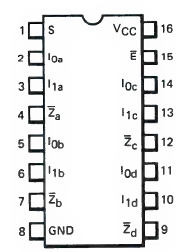
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — This device is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the device is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. It can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS158XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS158XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current I_0, I_1 E, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage I_0, I_1 E, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current I_0, I_1 E, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.8	8.0	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			20 24	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			16 16	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			13 11	ns	Fig. 1	

AC WAVEFORMS

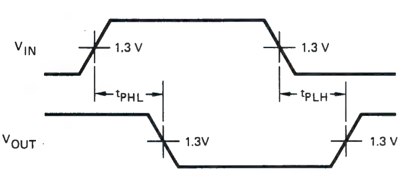


Fig. 1

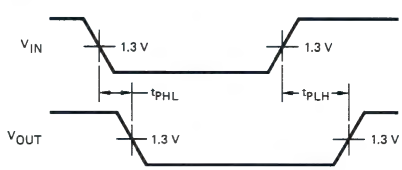


Fig. 2

5

F54LS/74LS160 • F54LS/74LS161
F54LS/74LS162 • F54LS/74LS163
BCD DECADE COUNTERS 4-BIT BINARY COUNTERS

DESCRIPTION—These devices are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting memory addressing, frequency division and other applications. The 54LS/74LS160 and 54LS/74LS162 count modulo 10 (BCD). The 54LS/74LS161 and 54LS/74LS163 count modulo 16 (binary).

The 54LS/74LS160 and 54LS/74LS161 have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The 54LS/74LS162 and 54LS/74LS163 have a Synchronous Reset (Clear) input that overrides all other control inputs; but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	54LS/74LS160	54LS/74LS161
Synchronous Reset	54LS/74LS162	54LS/74LS163

- **SYNCHRONOUS COUNTING AND LOADING**
- **TWO COUNT ENABLE INPUTS FOR HIGH-SPEED SYNCHRONOUS EXPANSION**
- **TERMINAL COUNT FULLY DECODED**
- **EDGE-TRIGGERED OPERATION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **FULLY TTL AND CMOS COMPATIBLE**

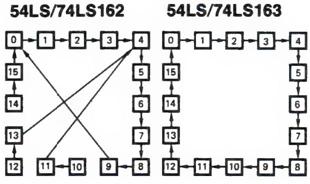
PIN NAMES / **LOADING** (Note a)

		HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.6 U.L.	0.3 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.6 U.L.	0.3 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.6 U.L.	0.3 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

STATE DIAGRAM

54LS/74LS160 **54LS/74LS161**
54LS/74LS162 **54LS/74LS163**



LOGIC EQUATIONS

Count Enable = CEP • CET • $\overline{PE}$

TC for 54LS/74LS160 & 54LS/74LS162 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3

TC for 54LS/74LS161 & 54LS/74LS163 = CET • Q_0 • Q_1 • Q_2 • Q_3

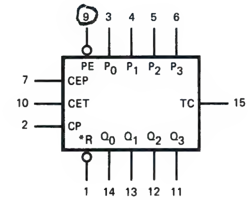
Preset = $\overline{PE}$ • CP + (rising clock edge)

Reset = $\overline{MR}$ (54LS/74LS160 & 54LS/74LS161)

Reset = $\overline{SR}$ • CP + (rising clock edge) (54LS/74LS162 & 54LS/74LS163)

NOTE:
The 54LS/74LS160 and 162 can be preset to any state, but will not count beyond nine. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

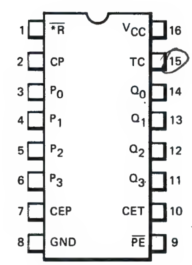
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

*$\overline{MR}$ for 54LS/74LS160 & 54LS/74LS161
*$\overline{SR}$ for 54LS/74LS162 & 54LS/74LS163

CONNECTION DIAGRAMS
DIP (TOP VIEW)



*$\overline{MR}$ for 54LS/74LS160 & 54LS/74LS161
*$\overline{SR}$ for 54LS/74LS162 & 54LS/74LS163

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — These devices are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset) in the 54LS/74LS160 and 54LS/74LS162 occur as a result of, and synchronous with, the LOW-to-HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs—Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW-to-HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the $\overline{PE}$ held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW-to-HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore be HIGH only for one count state.

The 54LS/74LS160 and 54LS/74LS162 count modulo-10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The 54LS/74LS161 and 54LS/74LS163 count modulo-16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the 54LS/74LS160 and 54LS/74LS161 is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the 54LS/74LS162 and 54LS/74LS163 acts as an edge-triggered control input, overriding CET, CEP, and $\overline{PE}$, and resetting the four counter flip-flops on the LOW-to-HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (_⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 54LS/74LS162 and 54LS/74LS163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

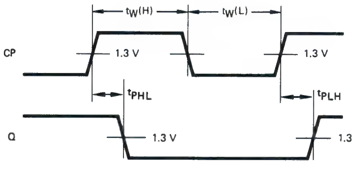
*Enter Input Voltage limit or Input Current limit is sufficient to protect the inputs.

logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

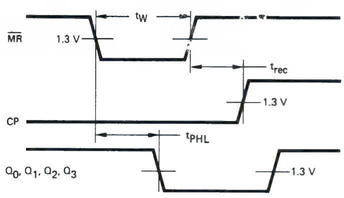
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS160XM 54LS161XM 54LS162XM 54LS163XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS160XC 74LS161XC 74LS162XC 74LS163XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

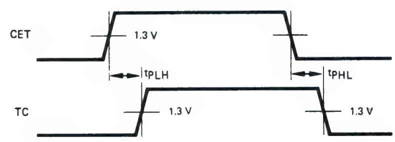
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN	TYP	MAX		

FAIRCHILD • F54LS/74LS160 • F54LS/74LS161 • F54LS/74LS162 • F54LS/74LS163

AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) state for the 54LS/74LS160 and 54LS/74LS162 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the 54LS/74LS161 and 54LS/74LS163.

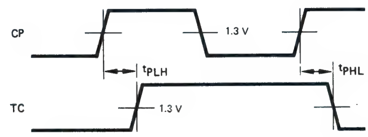


Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

Fig. 3

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) for the 54LS/74LS160 and 54LS/74LS162 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the 54LS/74LS161 and 54LS/74LS163.

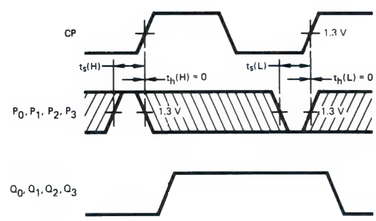


Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

Fig. 4

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

Fig. 5

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

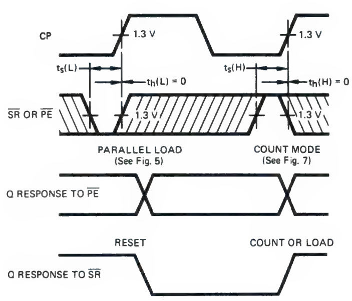
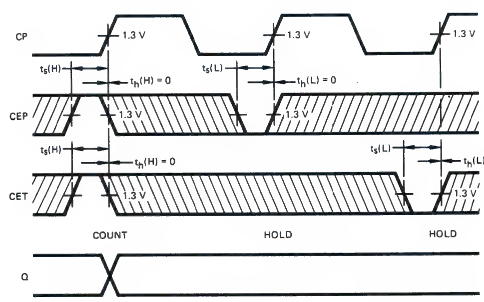


Fig. 6



Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H

Fig. 7

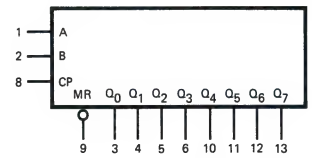
F54LS/74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION—The 54LS/74LS164 is a high-speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL products.

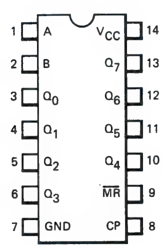
- **TYPICAL SHIFT FREQUENCY OF 35 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **GATED SERIAL DATA INPUT**
- **FULLY SYNCHRONOUS DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



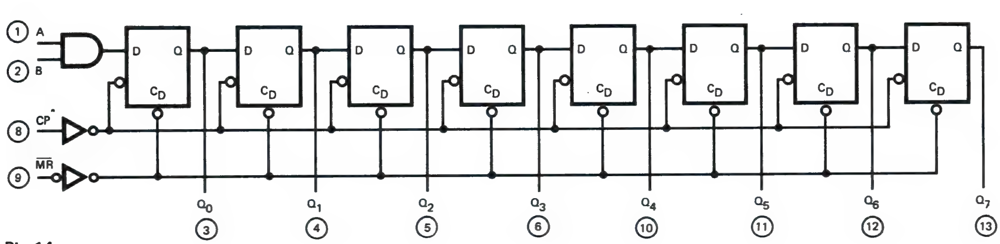
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION—This device is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs ($A \cdot B$) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS164XM	4.5 V	5.0 V	5.5 V	–55°C to +125°C
74LS164XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current (Note 6)			16	27	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
5. Not more than one output should be shorted at a time.
6. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Fig. 1	V_{CC} = 5 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to Outputs		17 21	27 32	ns	Fig. 1	
t_{PHL}	Propagation Delay, Negative-Going $\overline{MR}$ to Outputs		24	36	ns	Fig. 2	

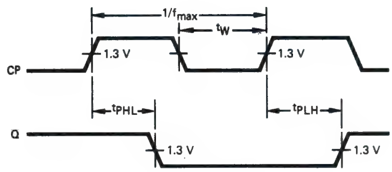
AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			ns	Fig. 3	V_{CC} = 5 V, C_L = 15 pF
t_h	Hold Time, A or B Input to Positive-Going CP	5			ns	Fig. 3	
t_WCP(H)	CP Pulse Width (HIGH)	20			ns	Fig. 1	
t_WCP(L)	CP Pulse Width (LOW)	20			ns	Fig. 1	
$t_W\overline{MR}$(L)	$\overline{MR}$ Pulse Width (LOW)	20			ns	Fig. 2	
t_{rec}	Recovery Time, Positive-Going $\overline{MR}$ to Positive-Going CP	20			ns	Fig. 2	

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $\overline{MR}$ = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

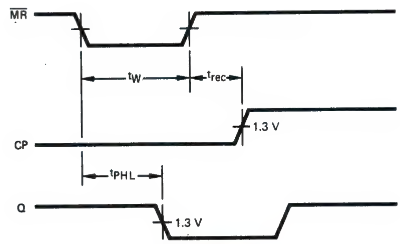


Fig. 2

DATA SET-UP AND HOLD TIMES

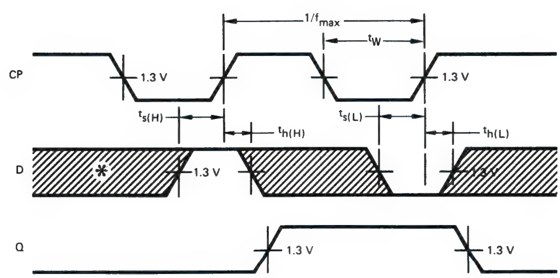


Fig. 3

F54LS/74LS173
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS173 is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the input Enable lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

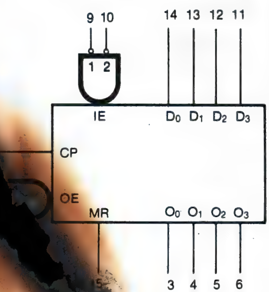
- **FULLY EDGE-TRIGGERED**
- **3-STATE OUTPUTS**
- **GATED INPUT AND OUTPUT ENABLES**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0 — D_3	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{IE}_1$, $\overline{IE}_2$	Input Enable (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset Input (Active HIGH)	0.5 U.L.	0.25 U.L.
O_0 — O_3	Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

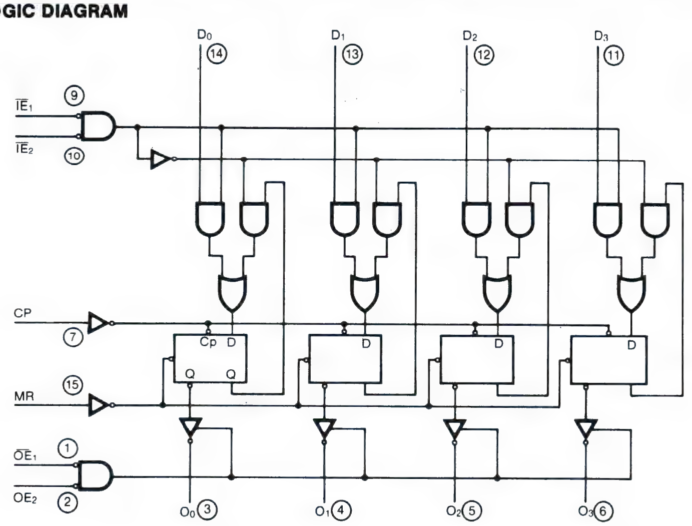
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



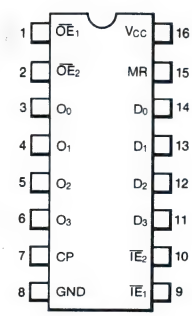
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS173	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS173	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package t[illegible] Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for p[illegible]vailable on this product.

[illegible] TRUTH TABLE

M[illegible]	[illegible]	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q_n
[illegible]	x	x	x	x	L
[illegible]	L	x	x	x	Q_n
[illegible]	↑	H	x	x	Q_n
L	↑	x	H	x	Q_n
L	↑	L	L	L	L
L	↑	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

When either $\overline{OE}_1$ or $\overline{OE}_2$ are HIGH, the output is in the off state (High Impedence); however this does not affect the contents or sequential operation of the register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = -1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = -2.6 mA	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				-20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				28	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°\,C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$
t_{PLH} t_{PHL}	Propagation Delay, CP T_0 Output		26 17	40 25	ns	Fig. 1	
t_{PHL}	Propagation Delay, MR T_0 Output		17	25	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		13	20	ns	Figs. 4, 5	$C_L = 15\ pF$
t_{PZL}	Output Enable Time to LOW Level		13	20	ns	Figs. 3, 5	$R_L = 2\ k\Omega$
t_{PLZ}	Output Disable Time from LOW Level		11	16	ns	Figs. 3, 5	$C_L = 5\ pF$
t_{PHZ}	Output Disable Time from HIGH Level		11	16	ns	Figs. 4, 5	$R_L = 2\ k\Omega$

AC SET-UP REQUIREMENTS: $T_A = 25°\,C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	[illegible]	TEST CONDITIONS	
$t_w(CP)$	Clock Pulse Width	17	11		[illegible]	Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$
$t_s(Data)$	Set-up Time, Data to Clock	10	7		[illegible]	[illegible] 1	
$t_h(Data)$	Hold Time, Data to Clock	10	7		ns		
$t_s(\overline{IE})$	Set-up Time, $\overline{IE}$ Control to Clock	17	11		ns	[illegible]	
$t_h(\overline{IE})$	Hold Time, $\overline{IE}$ Control to Clock	2	0		ns		
$t_w(MR)$	Master Reset Pulse Width	17	11		ns	Fig. [illegible]	
$t_{rec}(MR)$	Recovery Time, Master Reset to Clock	15	10		ns		

AC WAVEFORMS

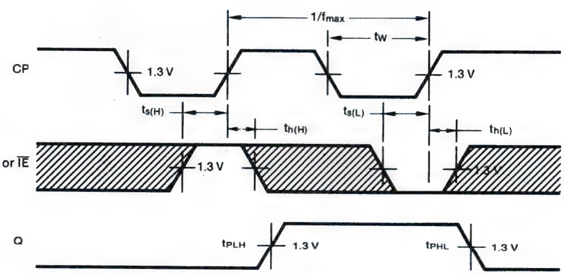


Fig. 1

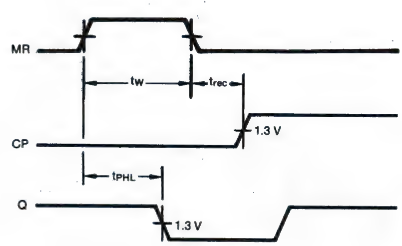


Fig. 2

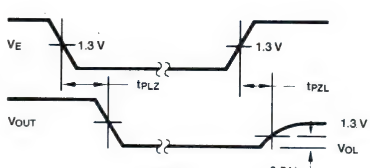


Fig. 3

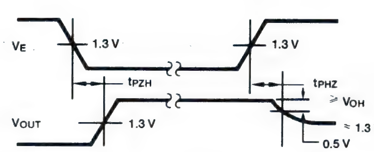


Fig. 4

AC LOAD CIRCUIT

Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

5

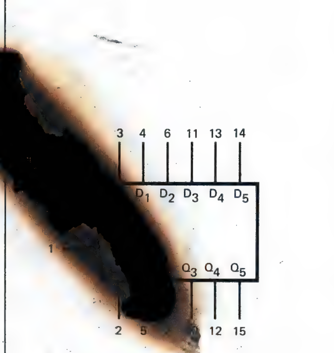
F54LS/74LS174

HEX D FLIP-FLOP

DESCRIPTION—The 54LS/74LS174 is a MSI high-speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERNATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



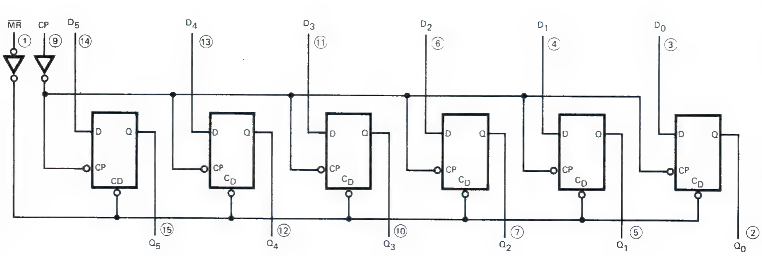
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

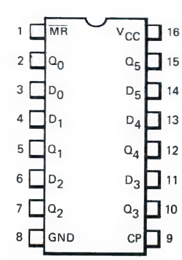
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — This device consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transfered to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The device useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS174XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS174XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			16	26	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

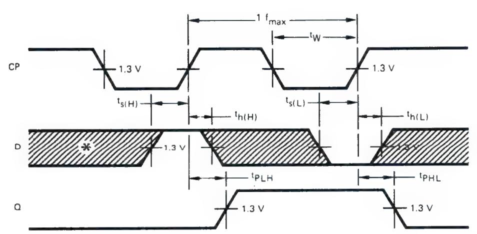
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		20	28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
$t_W CP$	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W \overline{MR}$	Minimum $\overline{MR}$ Pulse Width	12	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

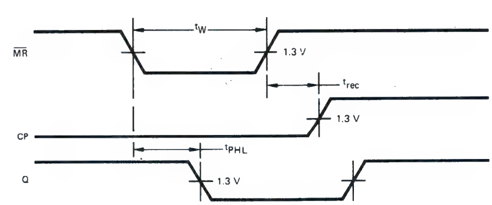


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

F54LS/74LS175
QUAD D FLIP-FLOP

DESCRIPTION—The 54LS/74LS175 is a MSI high-speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

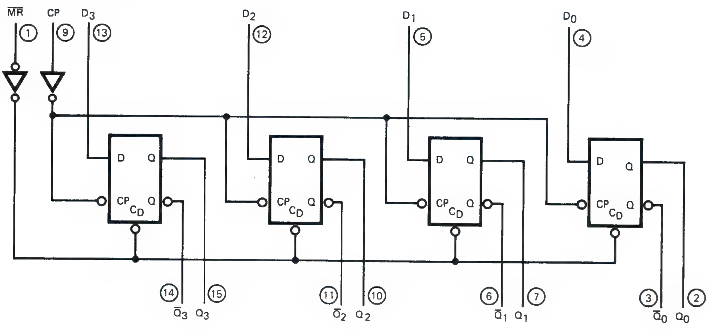
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

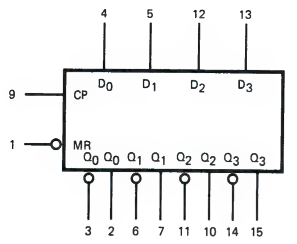
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



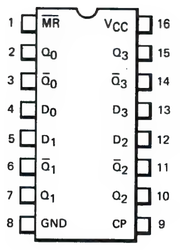
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

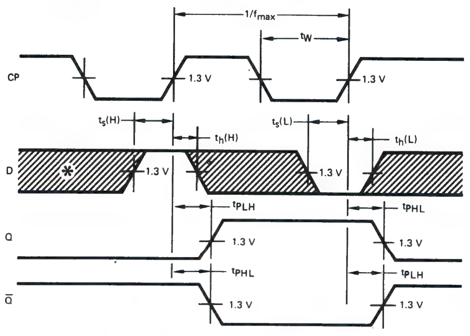
5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current D E				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage D E				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current D				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current					mA	V_{CC} = MAX

AC WAVEFORMS

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK

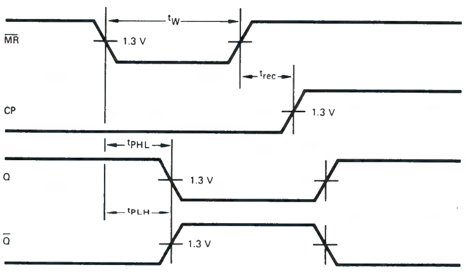


Fig. 2

5

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

FUNCTIONAL DESCRIPTION — This device consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

The device is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS175XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS175XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

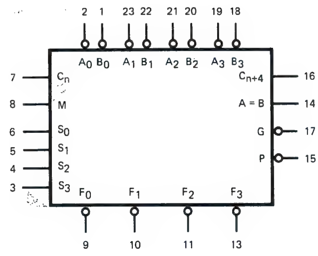
SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA	
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			11	18	mA	V_{CC} = MAX	

F54LS/74LS181
4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION—The 54LS/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**

LOGIC SYMBOL

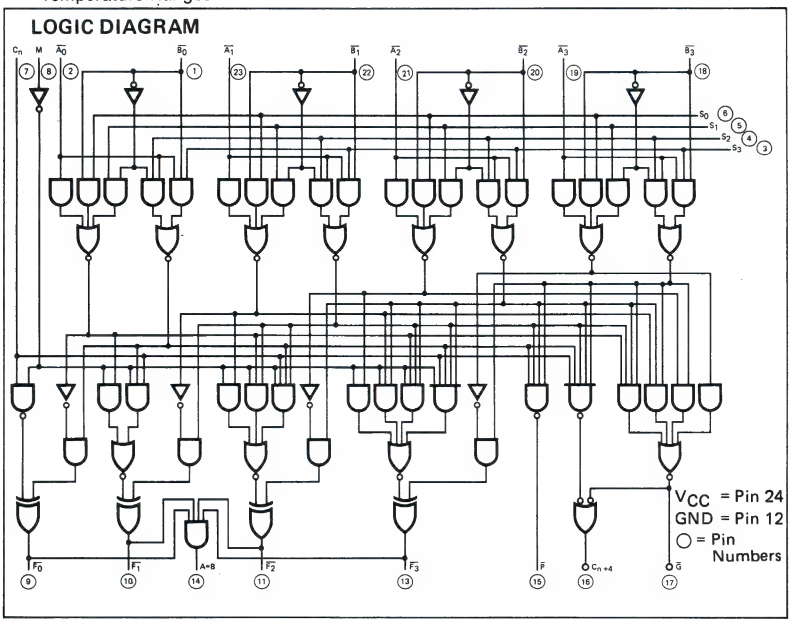


V_{CC} = Pin 24
GND = Pin 12

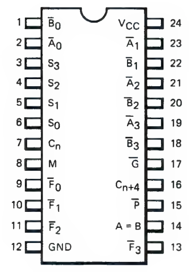
PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{A}_0$–$\overline{A}_3$, $\overline{B}_0$–$\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0–S_3	Function – Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C_n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0$–$\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
$\overline{G}$	Carry Generate (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION — The 54LS/74LS181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 54LS/74LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	$(A + \overline{B})$ plus A
H H H H	A	A	A	A minus 1

L = LOW Voltage Level

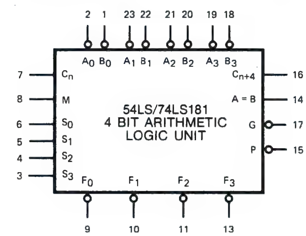
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

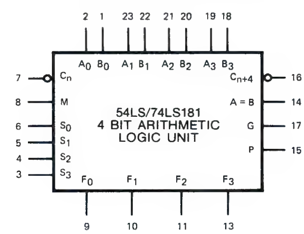
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS181XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS181XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA	
	Any Output except A=B	XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{OH}	Output HIGH Current A=B Output Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V	
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
	Output LOW Voltage Output $\overline{G}$			0.47	0.7	V	I_{OL} = 16 mA	
	Output LOW Voltage Output $\overline{P}$	XM		0.35	0.6	V	I_{OL} = 8.0 mA	
		XC		0.35	0.7			
I_{IH}	Input HIGH Current Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				 20 60 80 100	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				0.1 0.3 0.4 0.5	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				 −0.36 −1.08 −1.44 −2.0	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Condition A (Note 6)	XM		20	32	mA	V_{CC} = MAX	
		XC		20	34			
	Power Supply Current Condition B (Note 6)	XM		21	35			
		XC		21	37			

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. With outputs open, I_{CC} is measured for the following conditions:
   A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
   B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND

SYMBOL	PARAMETER	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\bar{F}$ Outputs)		26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)		29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)		32 26	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)		30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)		30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to any $\bar{F}$ Output)		32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to any $\bar{F}$ Output)		32 23	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{F}$ Outputs)		33 29	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to C_{n+4} Output)		38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to C_{n+4} Output)		41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to A = B Output)		50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V, R_L = 2 kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

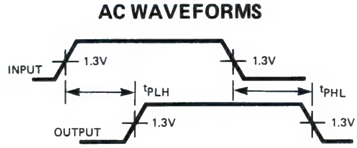


Fig. 4

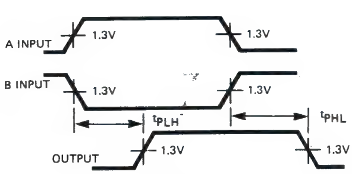


Fig. 5

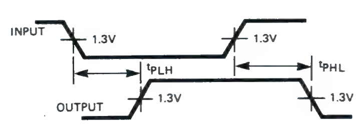


Fig. 6

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V

F54LS/74LS182

CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The 54LS/74LS182 is a high-speed Carry Lookahead Generator. It is generally used with the 54LS/74LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The carry lookahead generator is fully compatible with all members of the Fairchild TTL Family.

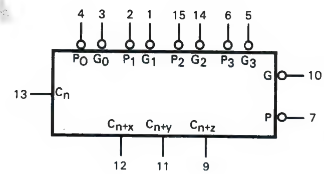
- **PROVIDES CARRY LOOKAHEAD ACROSS A GROUP OF FOUR ALUs**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES / **LOADING** (Note a)

PIN NAMES		HIGH	LOW
C_n	Carry Input	0.5 U.L.	0.25 U.L.
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active LOW) Inputs	3.5 U.L.	1.75 U.L.
$\overline{G}_1$	Carry Generate (Active LOW) Input	4.0 U.L.	2.0 U.L.
$\overline{G}_3$	Carry Generate (Active LOW) Input	2.0 U.L.	1.0 U.L.
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active LOW) Inputs	2.0 U.L.	1.0 U.L.
$\overline{P}_2$	Carry Propagate (Active LOW) Input	1.5 U.L.	0.75 U.L.
$\overline{P}_3$	Carry Propagate (Active LOW) Input	1.0 U.L.	0.5 U.L.
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.

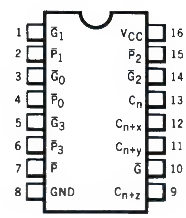
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH 1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



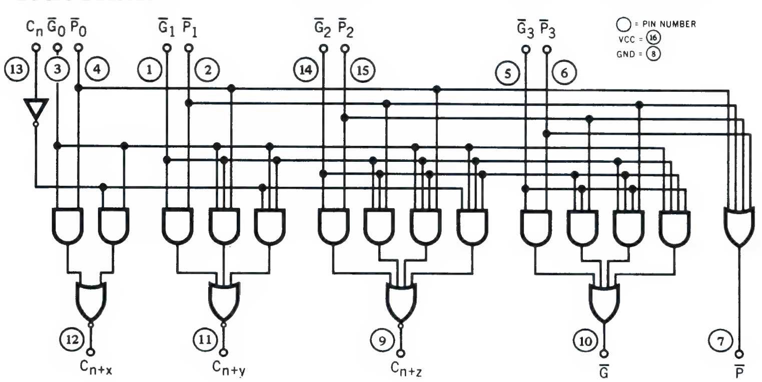
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



5

FUNCTIONAL DESCRIPTION—The 54LS/74LS182, carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 54LS/74LS182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_2G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Also, the 54LS/74LS182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS182XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS182XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN	I_{IN} = −18 mA
V_{OH}	Output HIGH voltage	XM	2.5			V	I_{OH} = -400 μA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7					
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8 mA	
I_{IH}	C_n				20	μA	V_{IN} = 2.7 V, V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				140	μA		
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				80	μA		
	$\overline{P}_2$				60	μA		
	$\overline{P}_3$				40	μA		
	$\overline{G}_1$				160	μA		
	C_n				.100	μA	V_{IN} = 10 V, V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				.700	μA		
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				.400	μA		
	$\overline{P}_2$				.300	μA		
	$\overline{P}_3$				.200	μA		
	$\overline{G}_1$				.800	μA		
I_{IL}	C_n				−0.4	mA	V_{IN} = 0.4 V, V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				−2.8	mA		
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				−1.6	mA		
	$\overline{P}_2$				−1.2	mA		
	$\overline{P}_3$				−0.8	mA		
	$\overline{G}_1$				−3.2	mA		
I_{OS}	Output Short-Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CCH}	Power Supply Current				12	mA	V_{CC} = MAX	
I_{CCL}					16			

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF, RL = 2 kΩ

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})		13 16		ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5 V Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})		9 12.5		ns	$\overline{P}_x$ = Gnd (If not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5 V, Fig. 2
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})		9 12.5		ns	$\overline{G}_x$ = 4.5 V (If not under test), $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, Fig. 2
t_{PLH} t_{PHL}	($\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$ or $\overline{P}$)		9 12.5		ns	$\overline{P}_x$ = Gnd (If not under test), $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = \overline{G}_3 = C_n$ = 4.5 V, Fig. 1
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ or $\overline{G}_3$ to $\overline{G}$)		26 8		ns	$\overline{G}_x$ = 4.5 V (If not under test), $\overline{P}_1 = \overline{P}_2 = \overline{P}_3$ = Gnd, Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{P}$)		20 8.5		ns	$\overline{P}_x$ = Gnd (If not under test), Fig. 1

AC WAVEFORMS

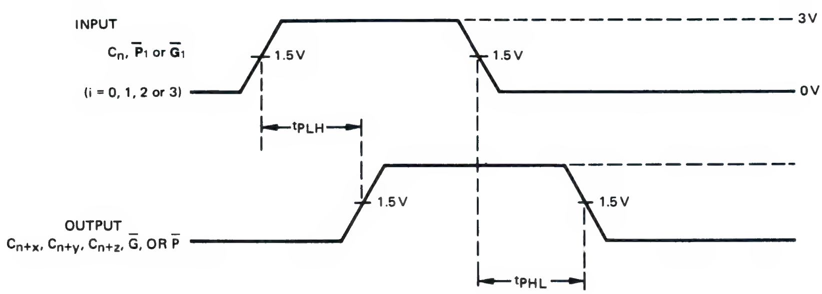


Fig.1

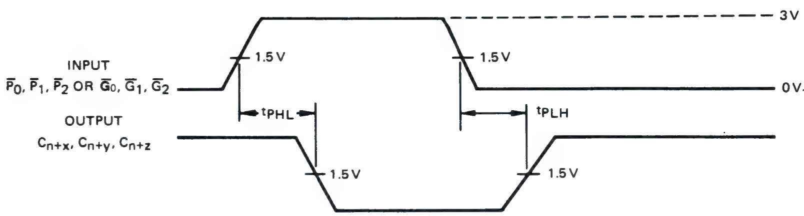


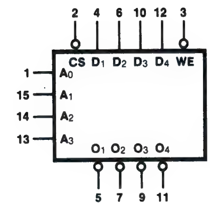
Fig. 2

F54LS189/74LS189
64-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS189 is a high-speed, low-power 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS.**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

5

PIN NAMES

AN	Address Input
$\overline{CS}$	Chip Select (active LOW) Input
D_n	Data Input
$\overline{O}_n$	Data (inverted) Output
$\overline{WE}$	Write Enable (active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	H	Write	HIGH Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	HIGH Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

F54LS/74LS190 • F54LS/74LS191

PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

DESCRIPTION—The 54LS/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the 54LS/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

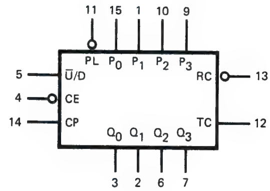
- **LOW POWER . . . 90 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 35 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **COUNT ENABLE AND UP/DOWN CONTROL INPUTS**
- **CASCADABLE**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}/D$	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{RC}$	Ripple Clock (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

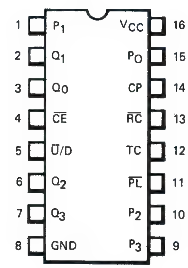
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



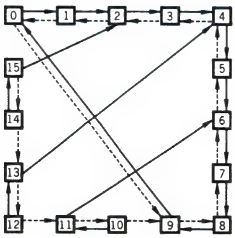
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



190

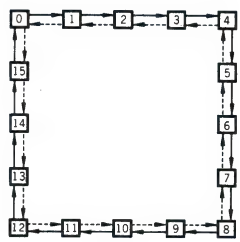
54LS/74LS190

UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{\overline{U}/D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U}/D)$

54LS/74LS191

UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{\overline{U}/D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U}/D)$

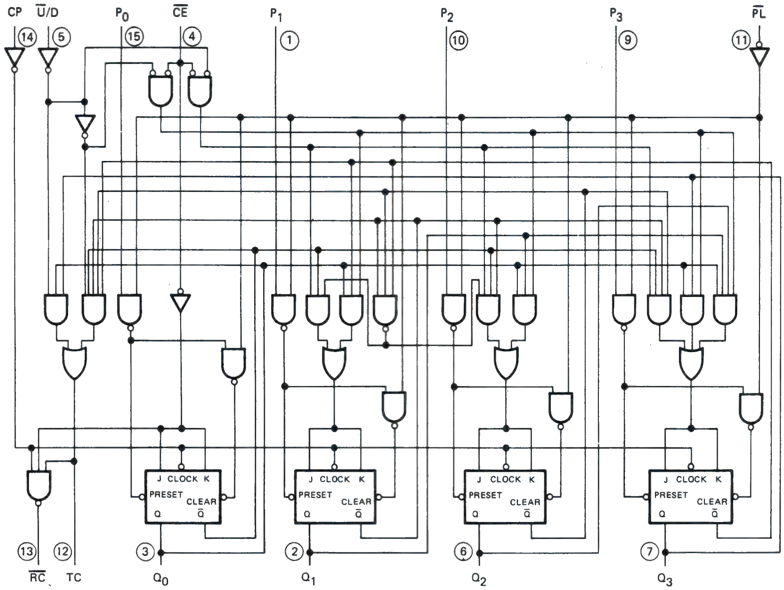
Count Up ——
Count Down ------



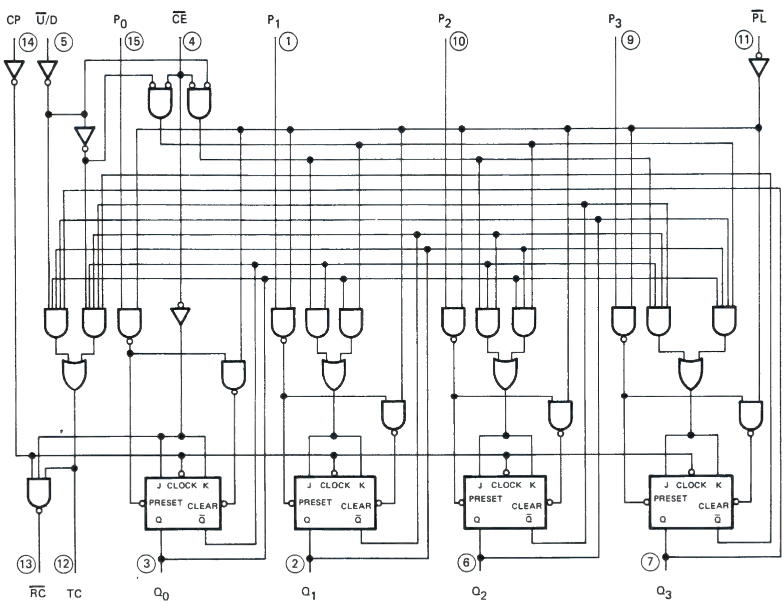
191

LOGIC DIAGRAMS

0000
0001
0010 B
0011
0100



DECADE COUNTER
54LS/74LS190



BINARY COUNTER
54LS/74LS191

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

5

FUNCTIONAL DESCRIPTION—The 54LS/74LS190 is a synchronous Up/Down BCD Decade Counter and the 54LS/74LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of these devices are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0—P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the 54LS/74LS190, 15 for the 54LS/74LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ TRUTH TABLE

INPUTS			$\overline{RC}$
$\overline{CE}$	TC*	CP	OUTPUT
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition
⊔ = LOW Pulse

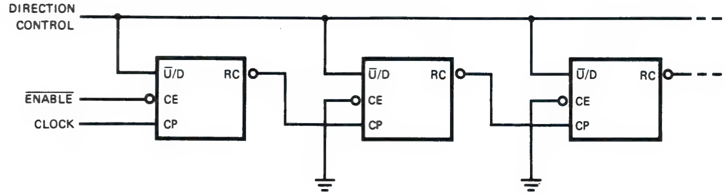


Fig. a) n-stage counter using ripple clock.

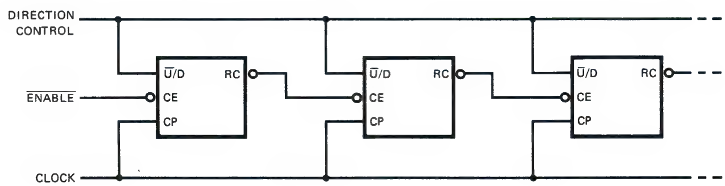


Fig. b) Synchronous n-stage counter using ripple carry/borrow.

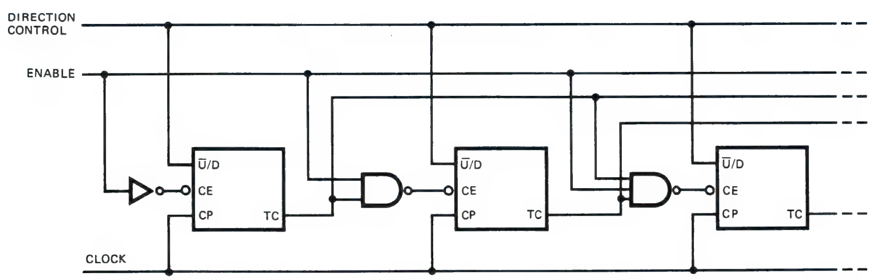


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

5

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS190XM 54LS191XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS190XC 74LS191XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Cermaic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current P_n, $\overline{PL}$, CP, $\overline{U}$/D $\overline{CE}$				20 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	P_n, $\overline{PL}$, CP, $\overline{U}$/D $\overline{CE}$				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current P_n, $\overline{PL}$, CP, $\overline{U}$/D $\overline{CE}$				−0.4 −1.08	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			20	35	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Count Enable ($\overline{CE}$) and the Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{CE}$ must occur only while the Clock is HIGH for conventional operation.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Max. Input Count Frequency	25	35		MHz	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs			24 36	ns	Fig. 1	
t_{PLH} t_{PHL}	CP Input to $\overline{RC}$ Output			20 24	ns	Fig. 2	
t_{PLH} t_{PHL}	CP Input to TC Output			42 52	ns	Fig. 1	
t_{PLH}* t_{PHL}*	$\overline{U}$/D Input to $\overline{RC}$ Output			45 45	ns	Fig. 7	
t_{PLH} t_{PHL}	$\overline{U}$/D Input to TC Output			33 33	ns	Fig. 7	
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs to $Q_0 - Q_3$ Outputs			22 50	ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output			33 50	ns	Fig. 4	
t_{PLH}* t_{PHL}	$\overline{CE}$ Input to $\overline{RC}$ Output			33 33	ns	Fig. 2	

*It is possible to get these timing relationships, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W	CP Pulse Width	20			ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{PL}$ Pulse Width	35			ns	Fig. 4	
t_sL	Set-Up Time LOW, Data to $\overline{PL}$	20			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			ns	Fig. 6	
t_sH	Set-Up Time HIGH, Data to $\overline{PL}$	20			ns	Fig. 6	
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			ns	Fig. 6	
t_{rec}	Recovery Time, $\overline{PL}$ to CP	20			ns	Fig. 5	
t_sL	Set-Up Time LOW, $\overline{CE}$ to Clock	20			ns	Fig. 8	
t_hL	Hold Time LOW, $\overline{CE}$ to Clock	0			ns	Fig. 8	

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

5

AC WAVEFORMS

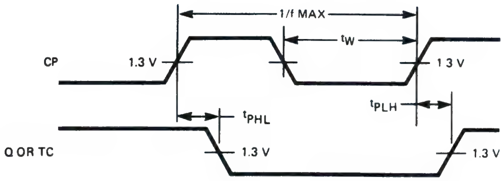


Fig. 1

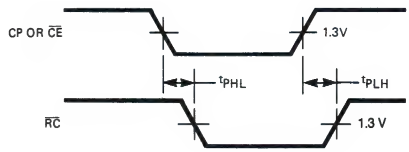
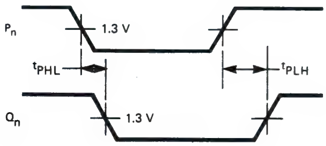


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

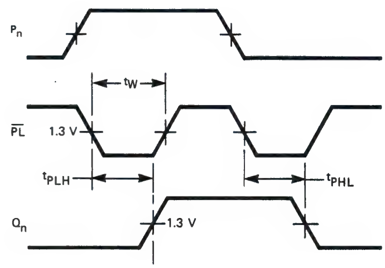


Fig. 4

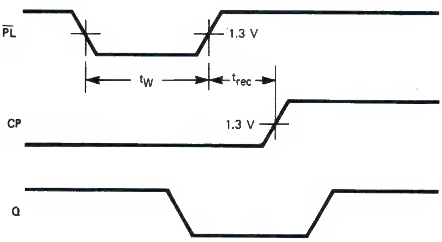
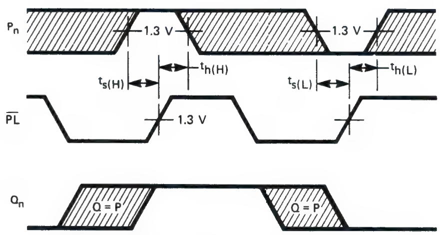


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

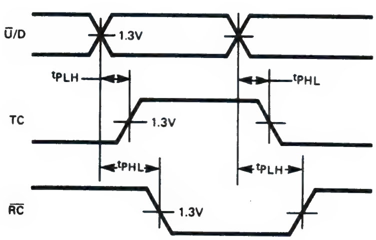


Fig. 7

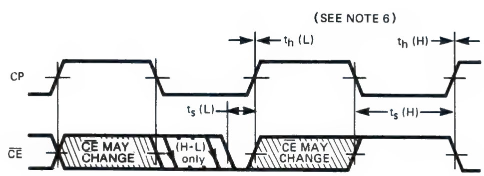


Fig. 8

F54LS/74LS192 • F54LS/74LS193

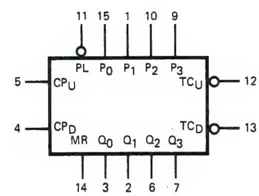
PRESETTABLE BCD/DECADE UP/DOWN COUNTER — PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION—The 54LS/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the 54LS/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- **LOW POWER ... 95 mW TYPICAL DISSIPATION**
- **HIGH SPEED ... 40 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



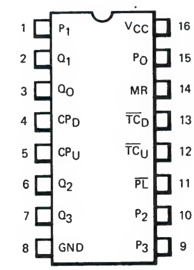
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

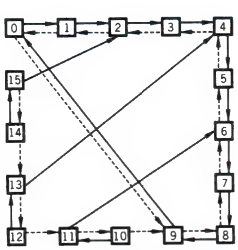
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



54LS/74LS192

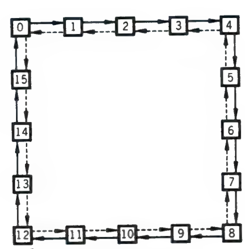
54LS/74LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

54LS/74LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

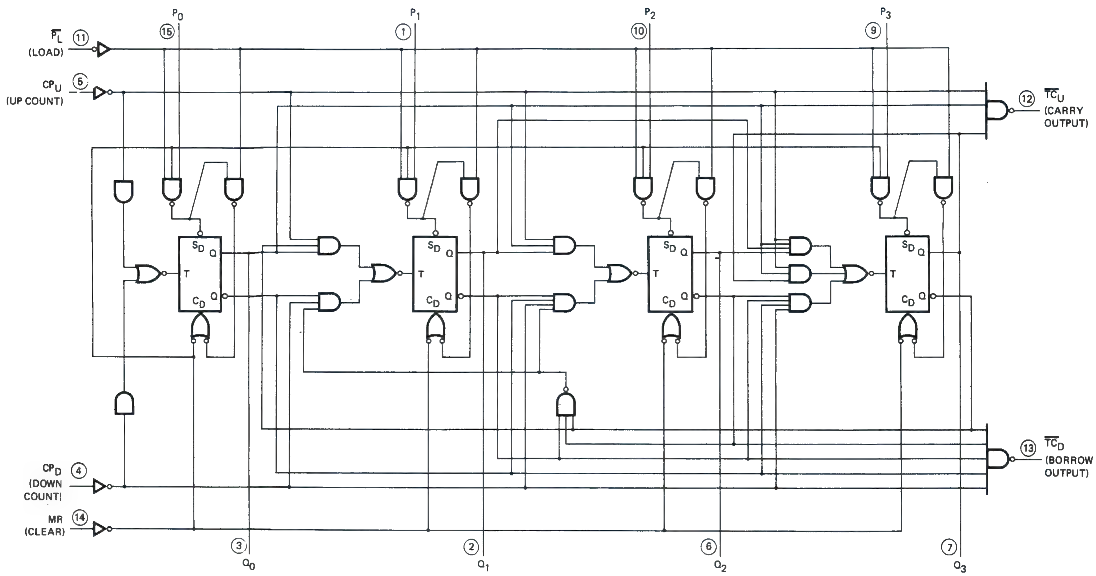
$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

COUNT UP ——
COUNT DOWN ------

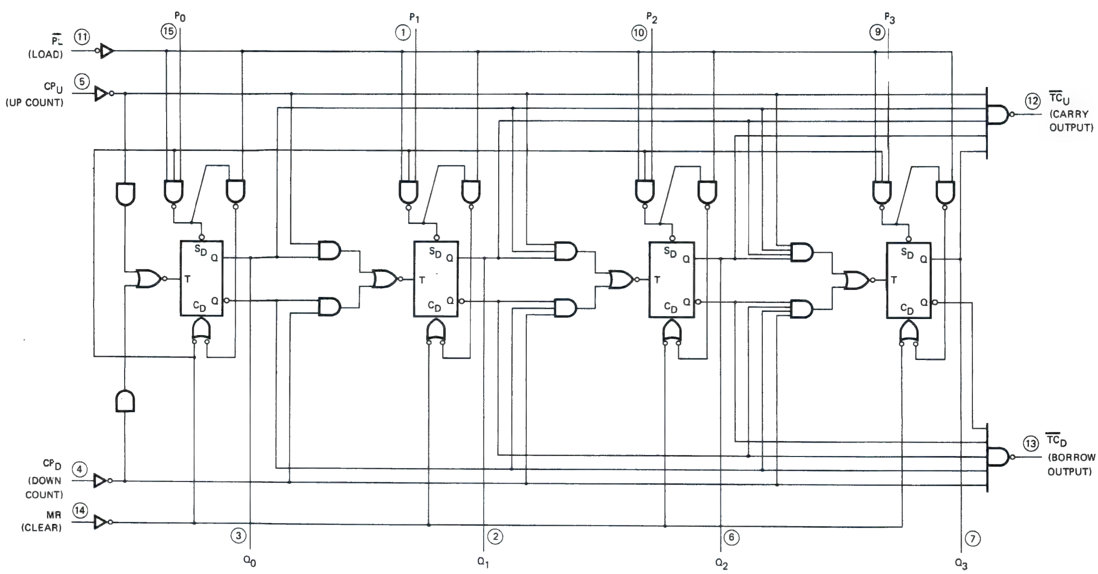


54LS/74LS193

LOGIC DIAGRAMS



54LS/74LS192



54LS/74LS193

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION—The 54LS/74LS192 and 54LS/74LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of these devices are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the 54LS/74LS192, 15 for the 54LS/74LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delaying by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset ($\overline{MR}$) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0 V
* Input Voltage (dc)	−0.5 V to 15 V
* Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

* Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS192XM 54LS193XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS192XC 74LS193XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			19	34	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, now shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS192 MIN	TYP	MAX	54LS/74LS193 MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Max Input Count Frequency	30	40		30	40		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		10 14	16 21		10 14	16 21	ns	Fig. 2	
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		10 15	16 22		10 15	16 22	ns	Fig. 2	
t_{PLH} t_{PHL}	CP_U or CP_D to Q_n Outputs		22 18	31 28		22 18	31 28	ns	Fig. 2	
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs $Q_0 - Q_3$ Outputs							ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		23 17	32 25		23 17	32 25	ns	Fig. 4	
t_{PHL}	$\overline{MR}$ Input to Any Output		17	25		17	25	ns	Fig. 7	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS192 MIN	TYP	MAX	54LS/74LS193 MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W	CP_U Pulse Width	17			17			ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	CP_D Pulse Width	17			17			ns	Fig. 1	
t_W	$\overline{PL}$ Pulse Width	15			15			ns	Fig. 4	
t_W	MR Pulse Width	15			15			ns	Fig. 7	
t_sL	Set-up Time LOW, Data to $\overline{PL}$	10			10			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			0			ns	Fig. 6	
t_sH	Set-up Time HIGH, Data to $\overline{PL}$	10			10			ns	Fig. 6	
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			0			ns	Fig. 6	
t_{rec}	Recovery Time, $\overline{PL}$ to CP							ns	Fig. 5	
t_{rec}	Recovery Time, $\overline{MR}$ to CP							ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transistion from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transistion from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transistion from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

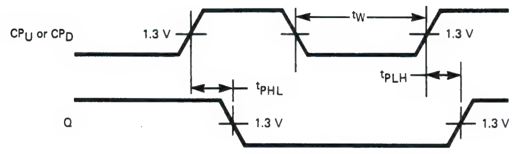


Fig. 1

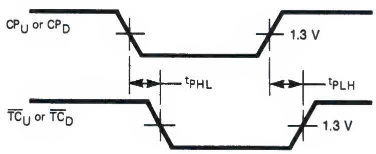
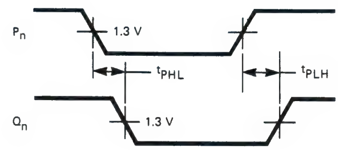


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

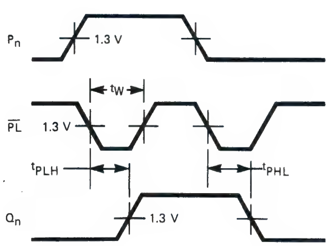


Fig. 4

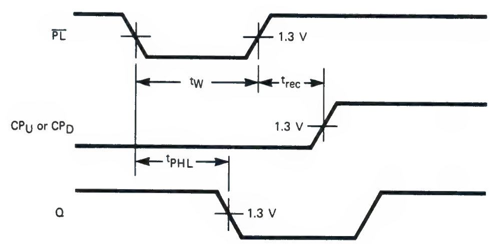
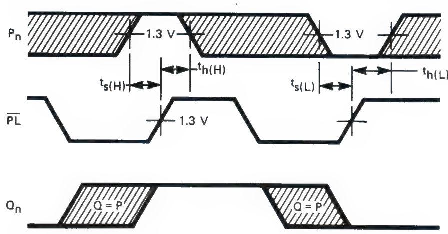


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

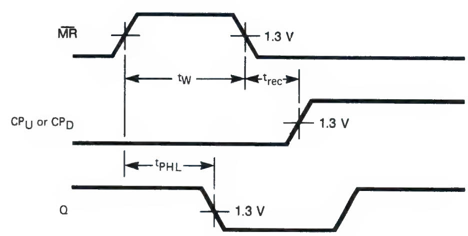


Fig. 7

F54LS/74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION—The 54LS/74LS194A is a High-Speed 4-Bit Bidirectional Universal Shift Register. As a high-speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. It is similar in operation to the 54LS/74LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL families.

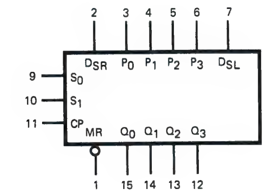
- **TYPICAL SHIFT FREQUENCY OF 40 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

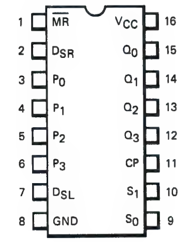
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL

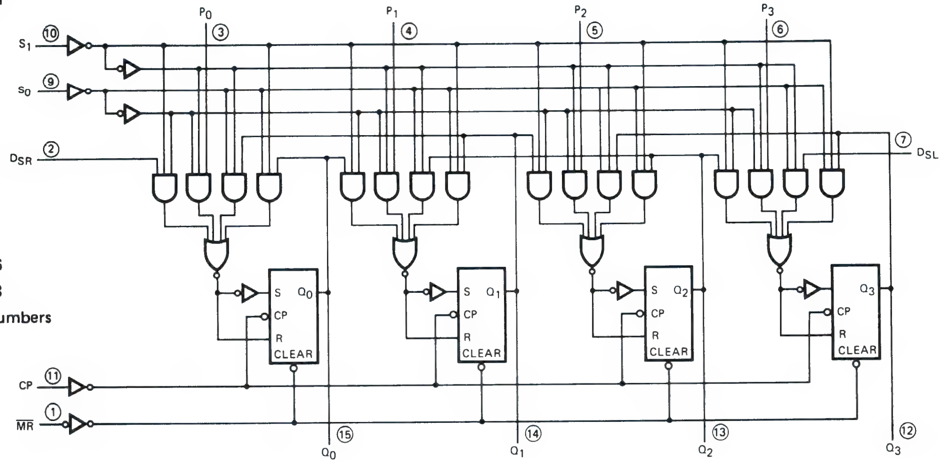


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the 4-Bit Bidirectional Shift Register. The device is similar in operation to the 54LS/74LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.
2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high-speed CPUs, or the memory buffer registers.
3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW-to-HIGH transition of the clock.
4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the device design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH-to-LOW clock transition.
2. D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

L = LOW Voltage Level
H= HIGH Voltage Level
X = Immaterial
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS194AXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS194AXC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA	
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			15	23	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		13 15	21 24	ns	Fig. 1	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		19	26	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$t_w(\overline{CP})$	Clock Pulse Width	17	5		ns	Fig. 1	$V_{CC} = 5.0$ V
t_s(Data)	Set-up Time, Data to Clock	16	10		ns	Fig. 3	
t_h(Data)	Hold Time, Data to Clock	0	-2		ns		
t_s(S)	Set-up Time, Mode Control to Clock	25	16		ns	Fig. 4	
t_h(S)	Hold Time, Mode Control to Clock	0	-12		ns		
$t_w(\overline{MR})$	Master Reset Pulse Width	12	10		ns	Fig. 2	
$t_{rec}(\overline{MR})$	Recovery Time Master Reset to Clock	18	10		ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

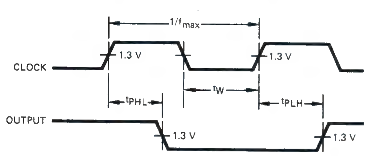
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

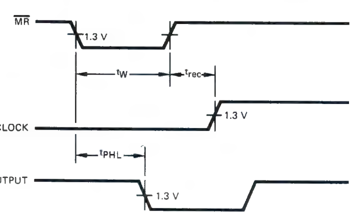
CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH AND f_{max}



OTHER CONDITIONS: $S_1 = L$, $\overline{MR} = H$, $S_0 = H$

Fig. 1

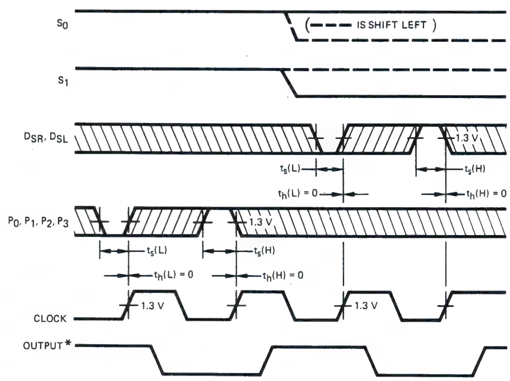
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



OTHER CONDITIONS: $S_0, S_1 = H$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 2

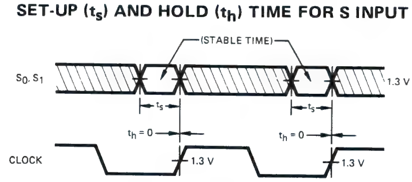
SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



OTHER CONDITIONS: $\overline{MR} = H$
*D_{SR} set-up time affects Q_0 only
D_{SL} set-up time affects Q_3 only

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT



OTHER CONDITIONS: $\overline{MR} = H$

Fig. 4

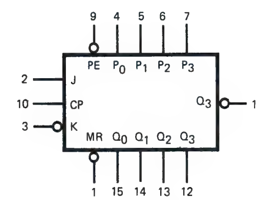
F54LS/74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION—The 54LS/74LS195A is a high-speed 4-Bit Shift Register offering typical shift frequencies of 40 MHz. It is useful for a wide variety of register and counting applications. The device is pin and functionally identical to the 9300, 93L00 and 93H00. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Fairchild TTL products.

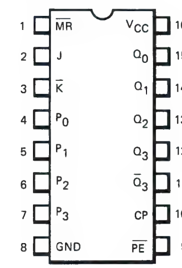
- **TYPICAL SHIFT RIGHT FREQUENCY OF 40 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



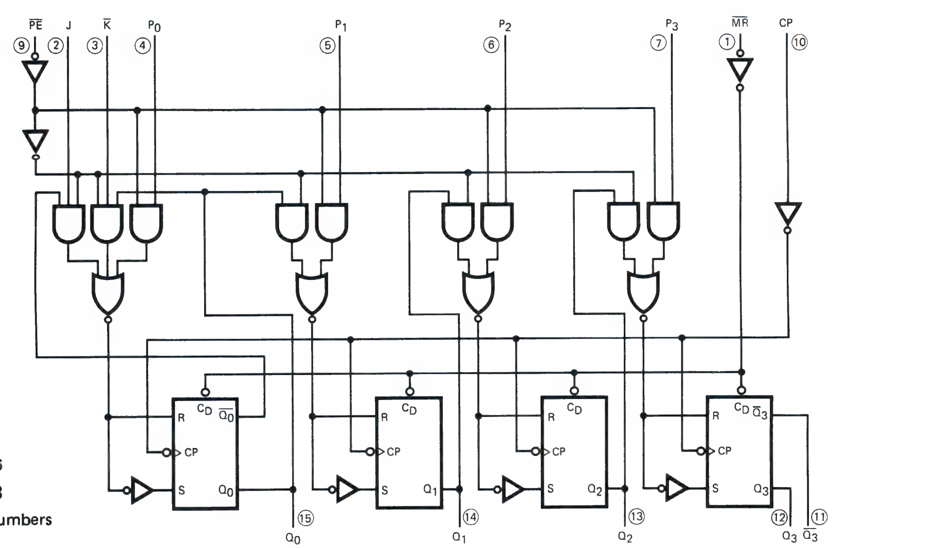
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The device has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins togethers. When the $\overline{PE}$ is LOW, the 9LS195 appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the device utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW voltage levels
H = HIGH voltage levels
X = Immaterial
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS195AXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS195AXC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			14	21	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		16 17	21 24	ns	Fig. 1	
t_{PHL}	Propagation Delay, MR to Output		17	26	ns	Fig. 3	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	16	7		ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	15	11		ns	Fig. 2	
t_h(Data)	Hold Time, Data to Clock	0	-3		ns		
t_s($\overline{PE}$)	Set-up Time, $\overline{PE}$ Control to Clock	25	18		ns	Fig. 4	
t_h($\overline{PE}$)	Hold Time, $\overline{PE}$ Control to Clock	0	-7		ns		
t_W($\overline{MR}$)	Master Reset Pulse Width	12	8		ns	Fig. 3	
t_{rec}($\overline{MR}$)	Recovery Time Master Reset to Clock	20	3		ns		

5

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

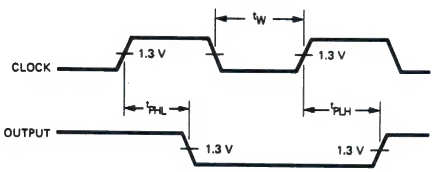
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

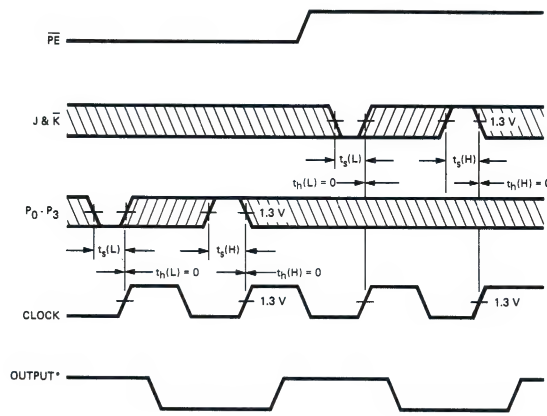
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 1

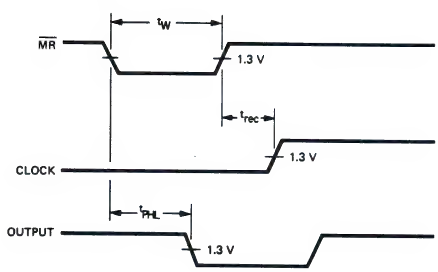
SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



CONDITIONS: $\overline{MR} = H$
*J and $\overline{K}$ set-up time affects Q_0 only

Fig. 2

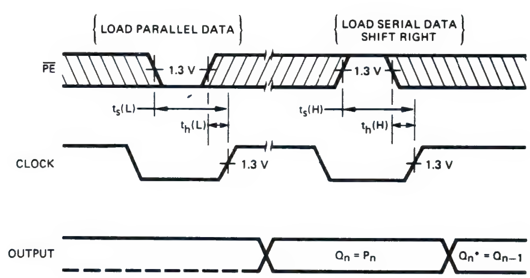
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



CONDITIONS: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



CONDITIONS: $\overline{MR} = H$
*Q_0 state will be determined by J and $\overline{K}$ inputs

Fig. 4

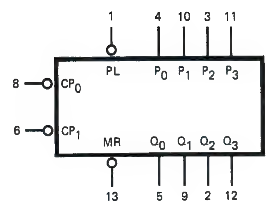
F54LS/74LS196 • F54LS/74LS197
4-STAGE PRESETTABLE RIPPLE COUNTERS

DESCRIPTION—The 54LS/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequences or in a bi-quinary mode producing a 50% duty cycle output. The 54LS/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used s 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

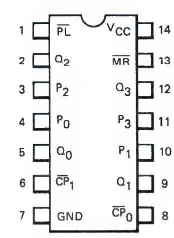
- **LOW POWER CONSUMPTION—TYPICALLY 80 mW**
- **HIGH COUNTING RATES—TYPICALLY 70 MHz**
- **CHOICE OF COUNTING MODES—BCD, BI-QUINARY, BINARY**
- **ASYNCHRONOUS PRESETTABLE**
- **ASYNCHRONOUS MASTER RESET**
- **EASY MULTISTAGE CASCADING**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



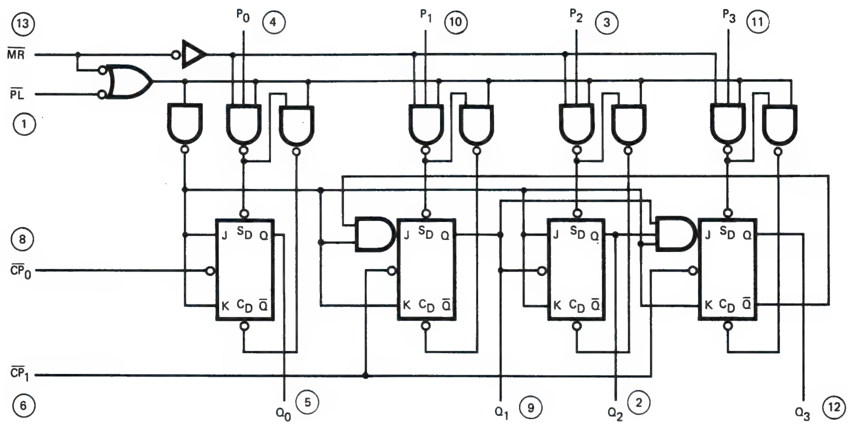
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

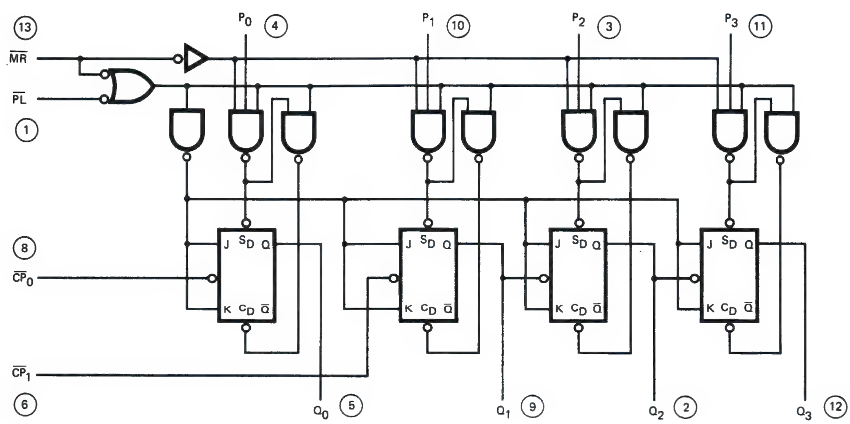
PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	1.0 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Notes b, c)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP}_1$.

LOGIC DIAGRAM



54LS/74LS196



54LS/74LS197

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION— These devices are asynchronously presettable decade and binary ripple counters. The 54LS/74LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the 54LS/74LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP}_1$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the 54LS/74LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

The 54LS/74LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

These devices have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P_0—P_3) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2: 9LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	‾|_	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
‾|_ = HIGH-to-LOW Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Temperature (Ambient) Under Bias	$-55^\circ C$ to $+125^\circ C$
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS196XM 54LS197XM	4.5 V	5.0 V	5.5 V	$-55^\circ C$ to $+125^\circ C$
74LS196XC 74LS197XC	4.75 V	5.0 V	5.25 V	$0^\circ C$ to $+70^\circ C$

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, $I_{OH} = -400\ \mu A$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				 20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP}_0$ $\overline{CP}_1$ (LS196) $\overline{CP}_1$ (LS197)				 −0.36 −0.72 −2.4 −2.8 −1.3	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			12	20	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, $T_A = 25^\circ C$.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS196 MIN	54LS/74LS196 TYP	54LS/74LS196 MAX	54LS/74LS197 MIN	54LS/74LS197 TYP	54LS/74LS197 MAX	UNITS	TEST CONDITIONS	
f_{max}	Input Count Frequency	45	60		50	75		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_0 Output		8.0 8.0	12 12		8.0 8.0	12 12	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		9.0 9.0	14 14		9.0 9.0	14 14	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		23 21	34 32		26 23	36 34	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		12 12	18 18		35 38	50 55	ns	Fig. 1	
t_{PLH} t_{PHL}	P_0, P_1, P_2, P_3 Inputs Q_0, Q_1, Q_2, Q_3 Outputs		10 24	15 35		10 24	15 35	ns	Fig. 2	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		15 24	24 35		15 24	24 35	ns	Fig. 3	
t_{PHL}	$\overline{MR}$ Input to Any Output		26	37		26	37	ns	Fig. 4	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS196 MIN	54LS/74LS196 TYP	54LS/74LS196 MAX	54LS/74LS197 MIN	54LS/74LS197 TYP	54LS/74LS197 MAX	UNITS	TEST CONDITIONS	
t_W	$\overline{CP}_0$ Pulse Width	12			10			ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	24			20			ns	Fig. 1	
t_W	$\overline{PL}$ Pulse Width	18			18			ns	Fig. 3	
t_W	$\overline{MR}$ Pulse Width	12			12			ns	Fig. 4	
t_sL	Set-up Time LOW Data to $\overline{PL}$	12			12			ns	Fig. 5	
t_hL	Hold Time LOW Data to $\overline{PL}$	6.0			6.0			ns	Fig. 5	
t_sH	Set-up Time HIGH Data to $\overline{PL}$	8.0			8.0			ns	Fig. 5	
t_hH	Hold Time HIGH Data to $\overline{PL}$	0			0			ns	Fig. 5	
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}$	16			16			ns	Fig. 4	
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	18			18			ns	Fig. 4	

DEFINITION OF TERMS:

SET-UP TIME (t_s)—is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h)—is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

RECOVERY TIME (t_{rec})—is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

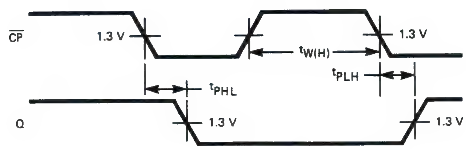
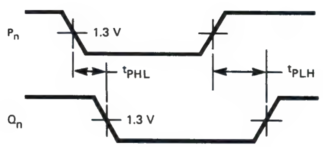


Fig. 1



NOTE: $\overline{PL}$ = LOW

Fig. 2

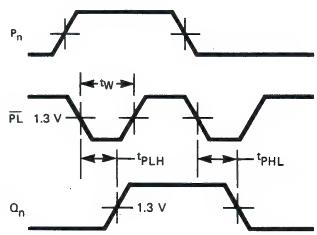


Fig. 3

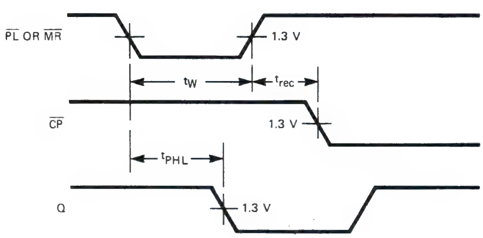
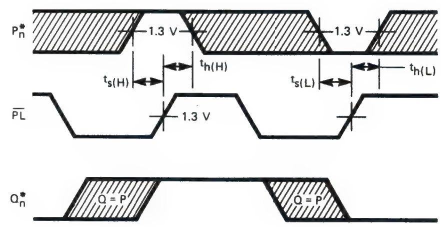


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

F54LS/74LS240 • F54LS/74LS241 • F54LS/74LS244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

DESCRIPTION—The 54LS/74LS240, 241 and 244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS**
- **3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS**
- **OUTPUTS SINK 40 mA AT V_{OL} = 0.5 V**
- **10 mA SOURCE CURRENT**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

TRUTH TABLES

54LS/74LS240

INPUTS		OUTPUT
$\overline{E}_1, \overline{E}_2$	D	
L	L	H
L	H	L
H	X	(Z)

54LS/74LS244

INPUTS		OUTPUT
$\overline{E}_1, \overline{E}_2$	D	
L	L	L
L	H	H
H	X	(Z)
H	X	(Z)

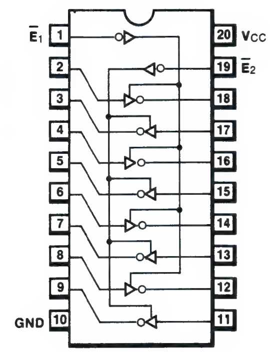
54LS/74LS241

INPUTS		OUTPUT	INPUTS		OUTPUT
E_1	D		$\overline{E}_2$	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)
H	X	(X)	L	X	(Z)

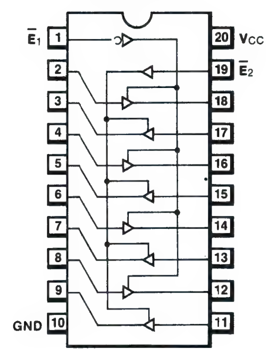
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

LOGIC AND CONNECTION DIAGRAMS
DIP (TOP VIEW)

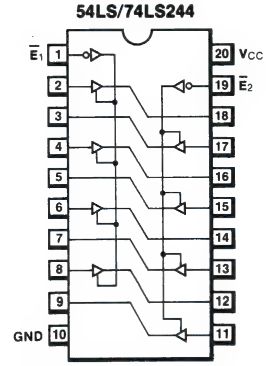
54LS/74LS240



54LS/74LS241



54LS/74LS244



ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS240XM, 54LS244XM 54LS241XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS240XC, 74LS244XC 74LS241XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −15 mA	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS240		29	50	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
		LS241, LS244		32	54			

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS240			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS241, 54LS/74LS244			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

AC WAVEFORMS

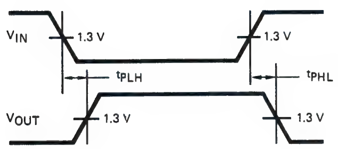


Fig.1

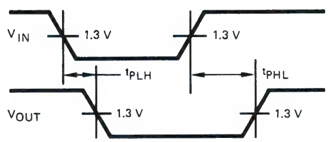


Fig. 2

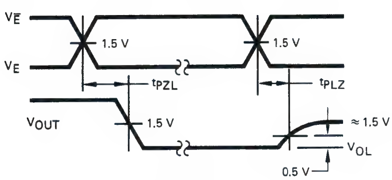


Fig. 3

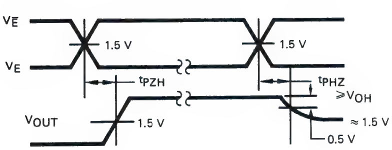
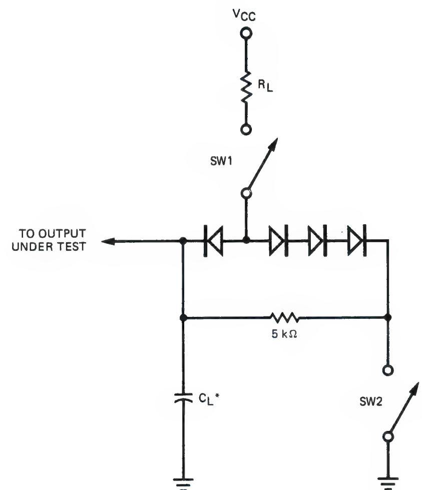


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

Fig. 5

5

F54LS/74LS242 • F54LS/74LS243

QUAD BUS TRANSCEIVER

DESCRIPTION—The 54LS/74LS242 and 54LS/74LS243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

TRUTH TABLES

54LS/74LS242

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	H	L	X	(Z)
L	H	L	L	X	(Z)
H	X	(Z)	H	L	H
H	X	(Z)	H	H	L

54LS/74LS243

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	L	L	X	(Z)
L	H	H	L	X	(Z)
H	X	(Z)	H	L	L
H	X	(Z)	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedence

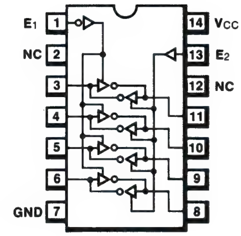
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

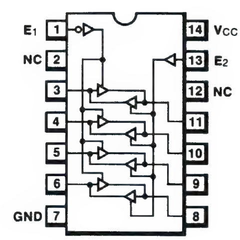
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC AND CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/74LS242



54LS/74LS243



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS242XM 54LS243XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS242XC 74LS243XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −15 mA	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS242		29	50	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
		LS243		32	54			

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS242			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS243			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

AC WAVEFORMS

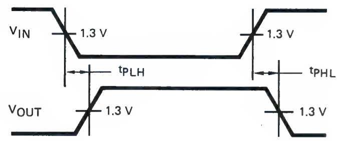


Fig.1

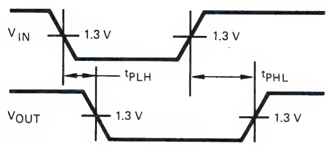


Fig. 2

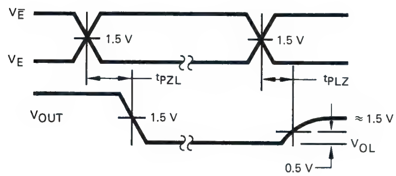


Fig. 3

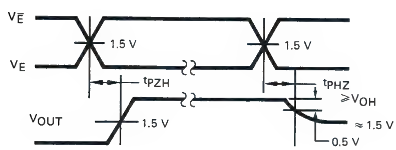
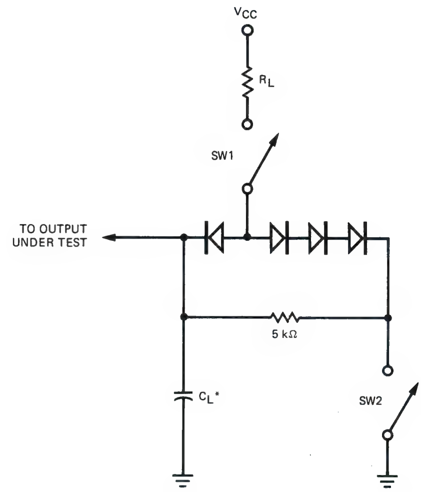


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

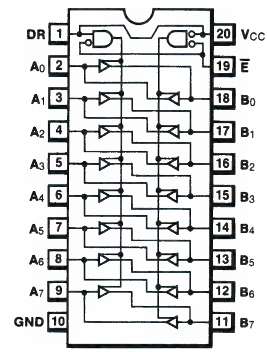
F54LS/74LS245

OCTAL BUS TRANSMITTER

DESCRIPTION—The 54LS/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

- **HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS245	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS245	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Output LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4				I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4				I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC			0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC			0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20 0.1	µA mA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 10V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4V	
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	Total, Output HIGH			60	mA	V_{CC} = MAX, Outputs Open	
		Total, Output LOW			85			
		Total at HIGH-Z			75			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

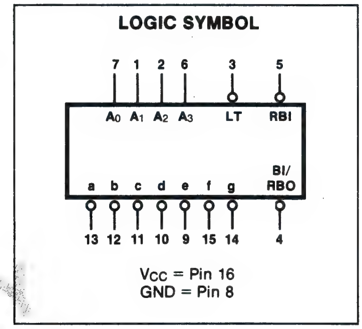
AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 18	ns	Figs. 1, 2	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			25	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

F54LS/74LS247

BCD TO 7-SEGMENT DECODER/DRIVER

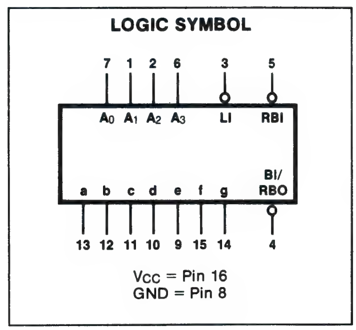
DESCRIPTION — The 54LS/74LS247 has active LOW open-collector outputs guaranteed to sink 12 mA (MILITARY) or 24 mA (COMMERICAL). It has the same electrical characteristics and pin connections as the 54LS/74LS47. The only difference is that the 54LS/74LS247 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.



F54LS/74LS248

BCD TO 7-SEGMENT DECODER

DESCRIPTION — The 54LS/74LS248 has active HIGH outputs with internal 2 kΩ pullup resistors. It has the same electrical characteristics and pin connections as the 54LS/74LS48. The only difference is that the 54LS/74LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

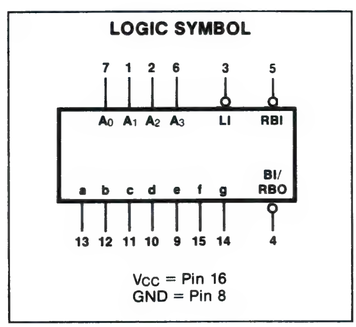


5

F54LS/74LS249

BCD TO 7-SEGMENT DECODER

DESCRIPTION — The 54LS/74LS249 has active HIGH open-collector outputs and is the 16-pin version of the 14 pin 54LS/74LS49. The 54LS/74LS249 incorporates the Lamp Test and BI/RBO inputs that are omitted in the 54LS/74LS49. Additionally, the 54LS/74LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.



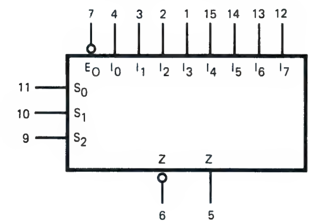
F54LS/74LS251

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS251 is a MSI high-speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

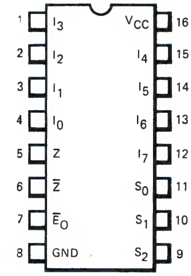
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



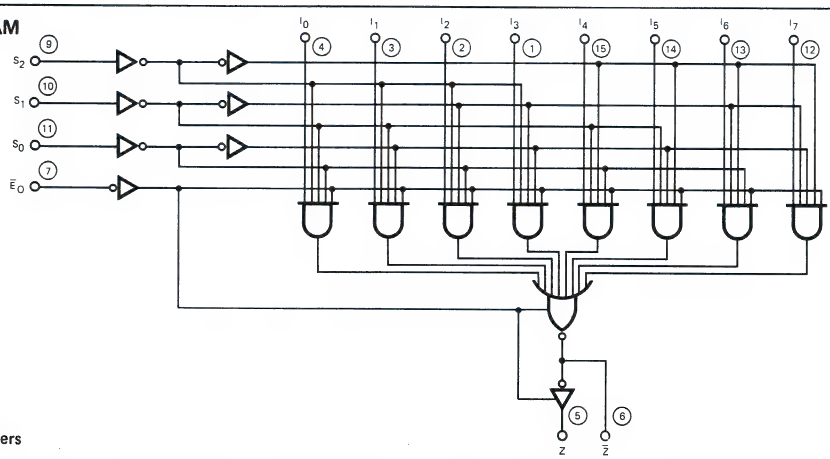
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_0$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{E}_O$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E}_O \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

$\overline{E}_O$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS251XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS251XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			6.1	10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs Off			7.1	12	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 33	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	45 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	27 23	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		12	20	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		17	25	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		12	20	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		17	25	ns	Figs. 4, 5	R_L = 2 kΩ

3-STATE AC WAVEFORMS

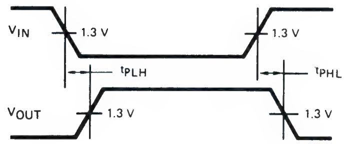


Fig. 1

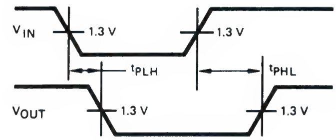


Fig. 2

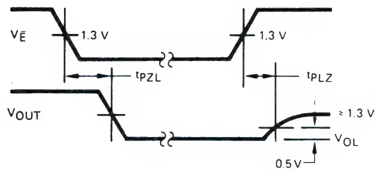


Fig. 3

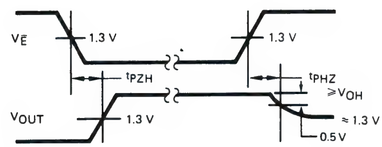
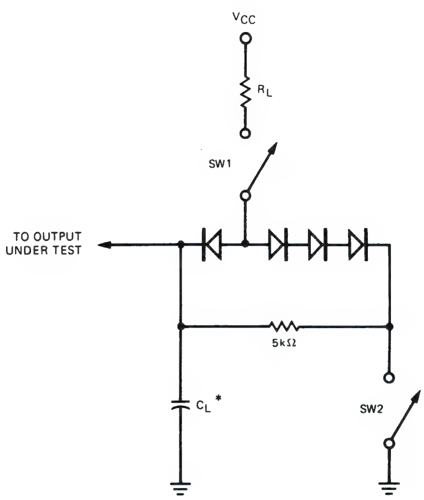


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

F54LS/74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS253 is a MSI Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{E}_O$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

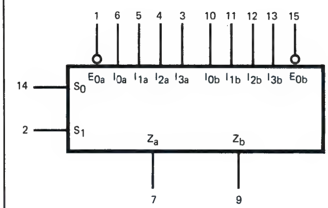
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

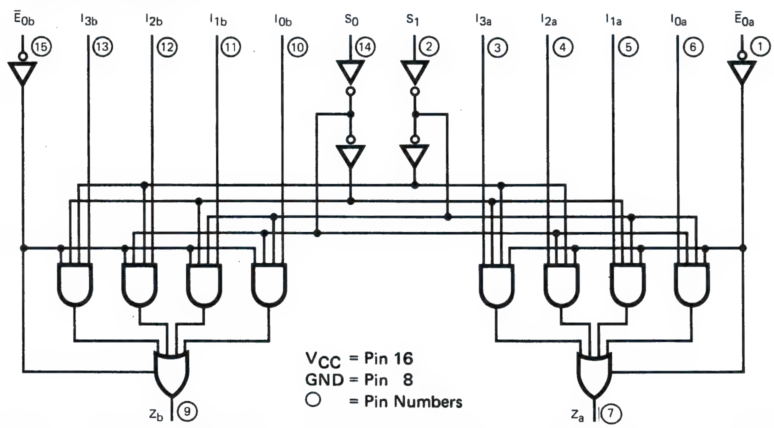
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL



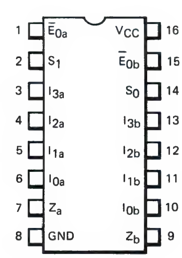
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — This device contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS253XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS253XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	29 24	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	18	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	32	ns	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	18	ns	Figs. 4, 5	

F54LS/74LS256

DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION—The F54LS/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{C}$). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

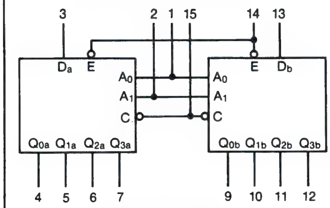
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{C}$) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{C}$ and $\overline{E}$ are both LOW. When $\overline{C}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q_0-Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$=LOW, $\overline{C}$=HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$=$\overline{C}$=HIGH).

- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **EASILY EXPANDABLE**
- **ACTIVE LOW COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

PIN NAMES		**LOADING** (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
D_a, D_b	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable Input (Active LOW)	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear Input (Active LOW)	0.5 U.L.	0.25 U.L.
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

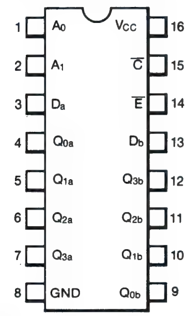
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



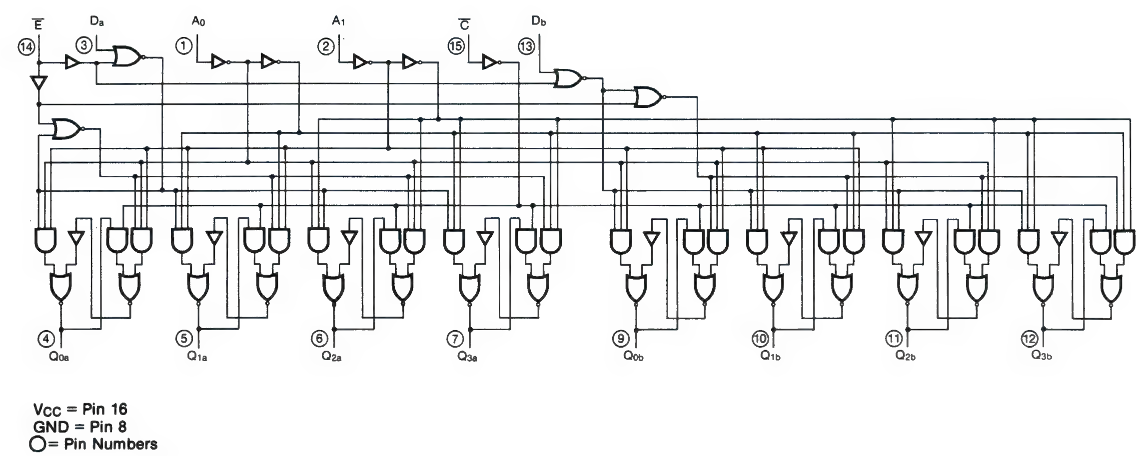
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
O= Pin Numbers

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
H	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable Latch
H	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	
H	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
H	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
H	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
H	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
H	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
H	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

H = High Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS256XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS256XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.1			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5		I_{OL} = 8.0 mA or V_{IL} per Truth Table
V_{IH}	Input HIGH Level		2.0			V	Guaranteed Input Logical HIGH Voltage for All Inputs
V_{IL}	Input LOW Level	XM			0.7	V	Guaranteed Input Logical LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{IL}	Input LOW Current A_0, A_1, $\overline{C}$, D_a, D_b E				 −0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current A_0, A_1, $\overline{C}$, D_a, D_b E				 20 40	μA	V_{CC} = MAX, V_{IN} = 2.4 V
I_{IH}	Input HIGH Current A_0, A_1, $\overline{C}$, D_a, D_b E				 0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{OS}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	36	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represents the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25° C, and MAX loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25° C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		20 16	27 24	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	30 20	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 2
t_{PLH} t_{PHL}	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		20 14	30 20	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 3
t_{PHL}	Turn-On Delay, Clear to Output		12	18	ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5

5

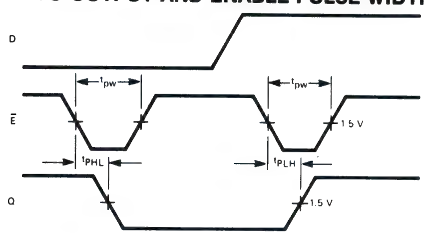
AC SET-UP REQUIREMENTS: $T_A = 25°$ C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_s (H)	Set-up Time HIGH, Data to Enable	20	13		ns	$V_{CC} = 5.0$ V Fig. 4
t_h (H)	Hold Time HIGH, Data to Enable	0	-7.0		ns	
t_s (L)	Set-up Time LOW, Data to Enable	15	7.0		ns	
t_h (L)	Hold Time LOW, Data to Enable	0	10		ns	
t_s (A-$\overline{E}$)	Set-up Time, Address to Enable (Note 6)	0	-7.0		ns	$V_{CC} = 5.0$ V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	12		ns	$V_{CC} = 5.0$ V Fig. 1

NOTES:
6. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
7. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

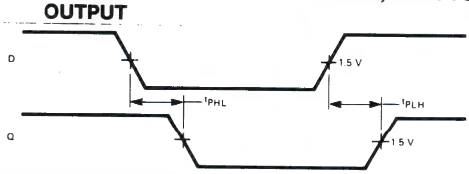
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



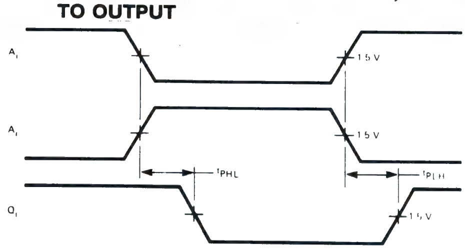
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



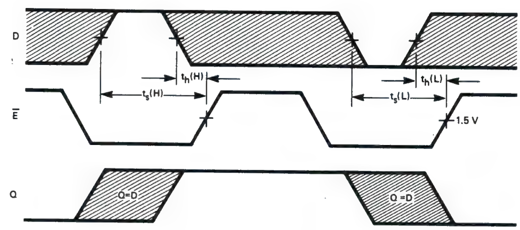
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



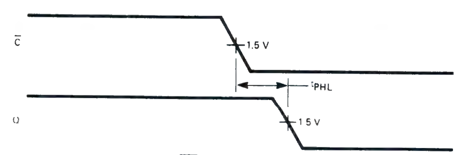
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME, DATA TO ENABLE



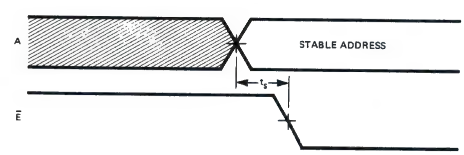
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SET-UP TIME, ADDRESS TO ENABLE (SEE NOTES 6 AND 7)



OTHER CONDITIONS: $\overline{C}$ = H

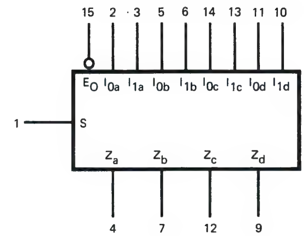
F54LS/74LS257

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS257 is a MSI Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



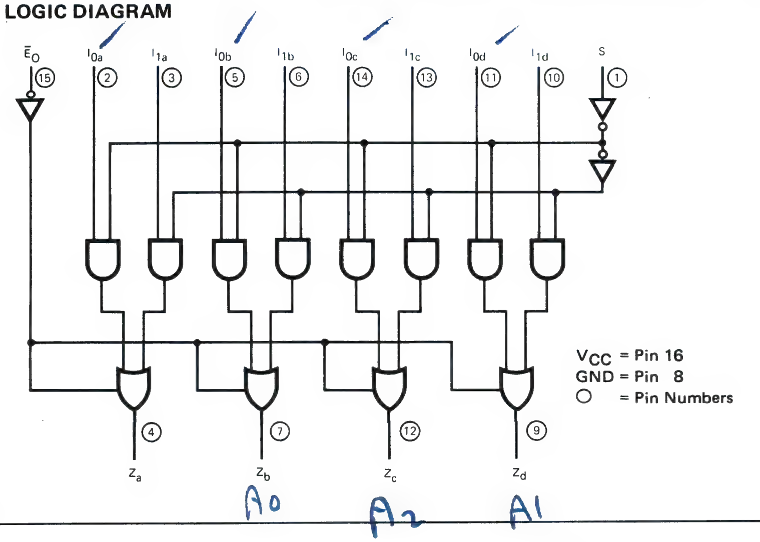
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Data Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5 (2.5) U.L.

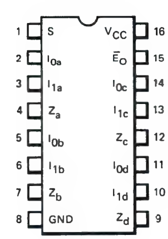
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — This device is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High impedance (off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS257XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS257XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x} S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x} S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x} S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				16		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				17		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 14	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level			28	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			24	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			22	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			14	ns	Figs. 4, 5	R_L = 2 kΩ

5

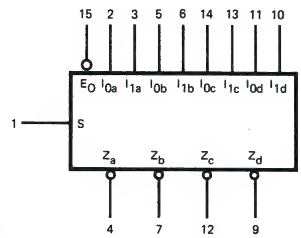
F54LS/74LS258

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS285 is a MSI Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



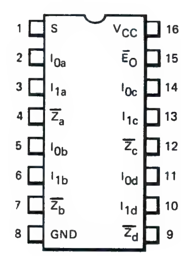
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Multiplexer Outputs (Active LOW) (Note b)	65(25) U.L.	5(2.5) U.L.

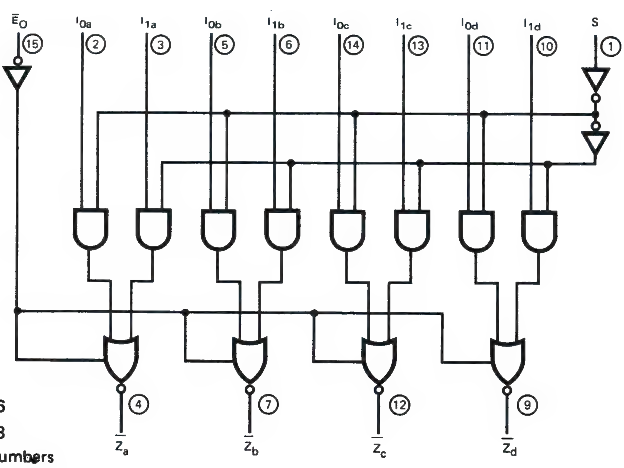
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select Input (S). When the Select Input is LOW, the I_O inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in inverted form.

The Quad 2-Input Multiplexer is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad \overline{Z}_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad \overline{Z}_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS258XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS258XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x} S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x} S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x} S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				7	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				14	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				19	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 18	ns	Fig. 1	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			30	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667
t_{PLZ}	Output Disable Time from LOW Level			30	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			25	ns	Figs. 4, 5	R_L = 667

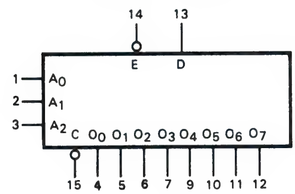
F54LS/74LS259

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The 54LS/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

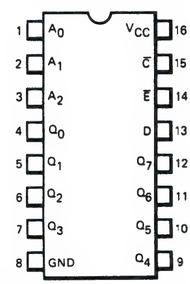
- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

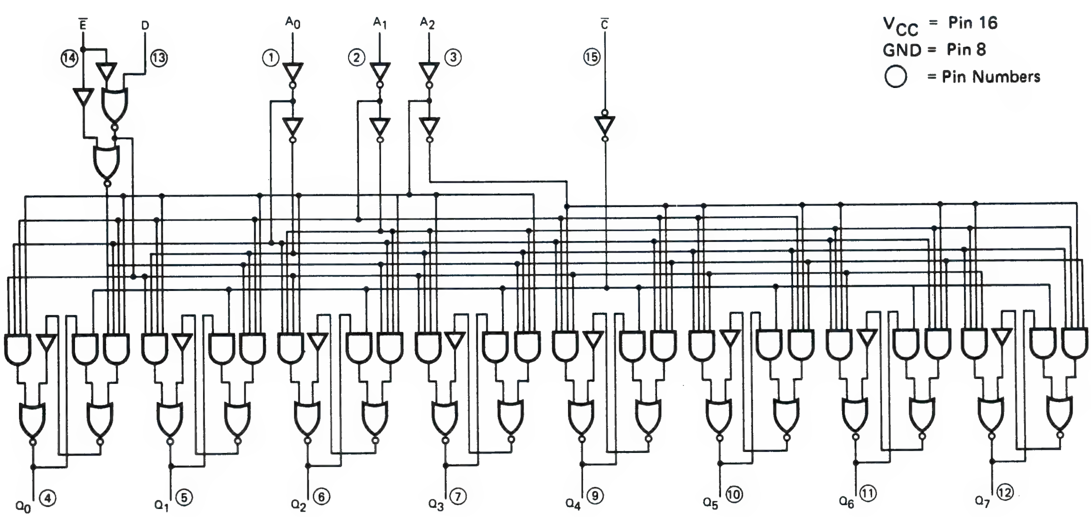
CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES		LOADING (Note a) HIGH	LOW
A_0, A_1, A_2	Address Inputs	0.5 U.L.	0.25 U.L.
D	Data Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 54LS/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 54LS/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations of the 54LS/74LS259.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	MODE
						PRESENT OUTPUT STATES								
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮		⋮					⋮					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	→	→	→	→	Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}	→	→	→	→	→	
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}	→	→	→	→	→	
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
⋮	⋮	⋮		⋮				⋮						
H	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	Q_{N-1}	H	

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS259XM	4.5 V	5.0 V	5.5 V	-55° C to 125° C
74LS259XC	4.75 V	5.0 V	5.25 V	0° C to 70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.4	3.1				
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA	
V_{IH}	Input HIGH Level		2.0			V	Guaranteed Input Logical HIGH Voltage for All Inputs	
V_{IL}	Input LOW Level	XM			0.7	V	Guaranteed Input Logical LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = 18 mA	
I_{IL}	Input LOW Current A_0, A_1, A_2, D, C, E				 −0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current A_1, A_2, A_3, D, C, E				 20 40	μA	V_{CC} = MAX, V_{IN} = 2.4 V	
I_{IH}	Input HIGH Current A_1, A_2, A_3, D, C, E				 0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{OS}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			20	36	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and max loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
t_{PLH}	Turn-Off Delay, Enable to Output		20	27	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Enable to Output		16	24	ns	Fig. 1
t_{PLH}	Turn-Off Delay, Data to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Data to Output		13	20	ns	Fig. 2
t_{PLH}	Turn-Off Delay, Address to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Address to Output		14	20	ns	Fig. 3
t_{PHL}	Turn-On Delay, Clear to Output		12	18	ns	V_{CC} = 5.0 V, C_L = 15pF Fig. 5

5

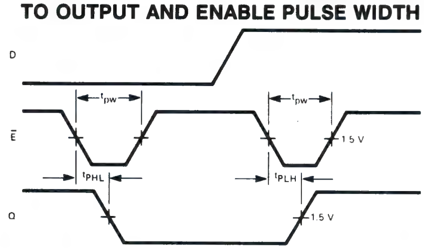
AC SET-UP REQUIREMENTS $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_s (H) t_h (H)	Set-up Time HIGH, Data to Enable Hold Time HIGH, Data to Enable	20 0	13 -7.0		ns ns	V_{CC} = 5.0 V Fig. 4
t_s (L) t_h (L)	Set-up Time LOW, Data to Enable Hold Time LOW, Data to Enable	15 0	7 10		ns ns	
t_s (A-$\overline{E}$)	Set-up Time, Address to Enable (See Note 1)	0	-7.0		ns	V_{CC} = 5.0 V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	12		ns	V_{CC} = 5.0 V Fig. 1

NOTES:
1. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

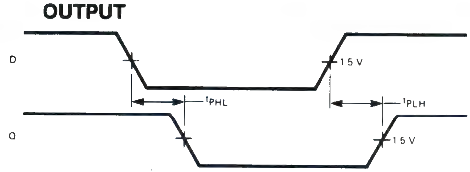
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



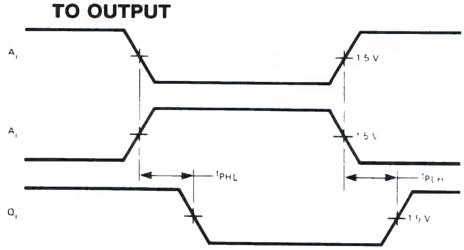
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



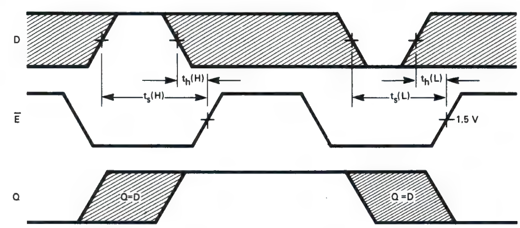
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



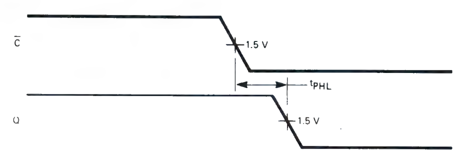
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME, DATA TO ENABLE



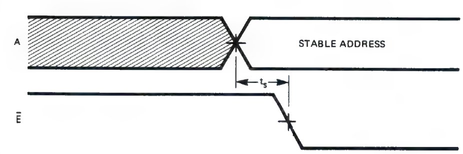
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

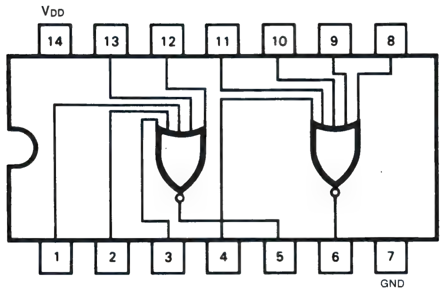
Fig. 6 SET-UP TIME, ADDRESS TO ENABLE (SEE NOTES 1 AND 2)



OTHER CONDITIONS: $\overline{C}$ = H

F54/74LS260

DUAL 5-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS260XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS260XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F = Flatpak, D = Ceramic Dip, P = Plastic Dip

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	XM, XC	2.5	3.4			V_{CC} = MIN, I_{OH} = -400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH				4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW				5.5	mA	V_{CC} = MAX, Inputs Open

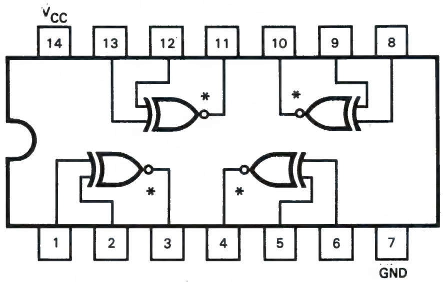
AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	6.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS266

QUAD 2-INPUT EXCLUSIVE NOR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS266XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS266XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current				100	µA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			8.0	13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

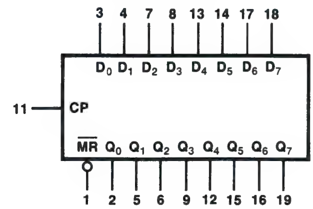
F54LS/74LS273

8-BIT REGISTER WITH CLEAR

DESCRIPTION – The 54LS/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- **8-BIT HIGH SPEED REGISTER**
- **PARALLEL REGISTER**
- **COMMON CLOCK AND MASTER RESET**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



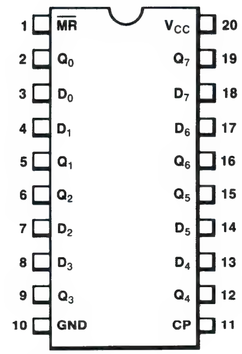
V_{CC} = Pin 20
GND = Pin 10

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
D_0–D_7	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0–Q_7	Register Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)

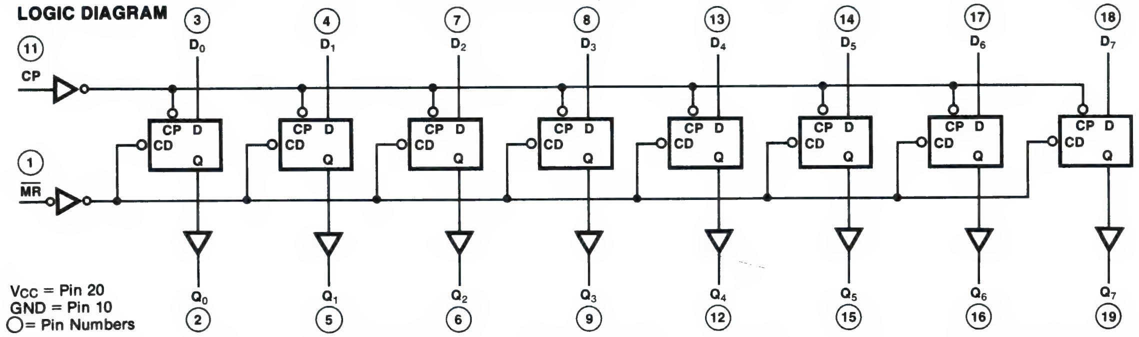


TRUTH TABLE

$\overline{MR}$	CP	D_x	Q_x
L	X	X	L
H	⎍	H	H
H	⎍	L	L

H = High Logic Level
L = Low Logic Level
X = Immaterial

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 54LS/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS273XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS273XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short-Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			17	28	mA	V_{CC} = MAX

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay , Clock to Output			20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output			28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1

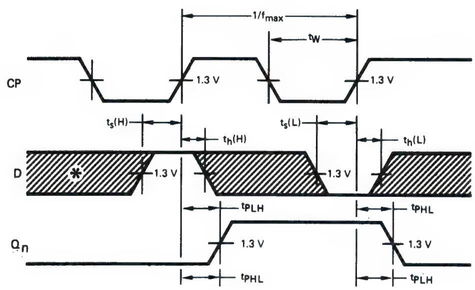
AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_wCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	15			ns	Fig. 2
$t_w\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	15	8		ns	Fig. 2

5

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

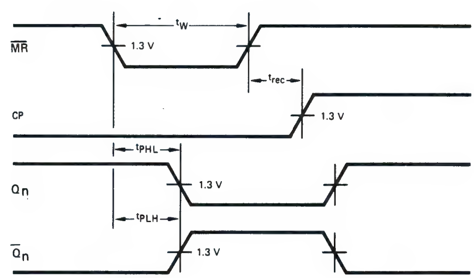


Fig. 2

DEFINITIONS OF TERMS:

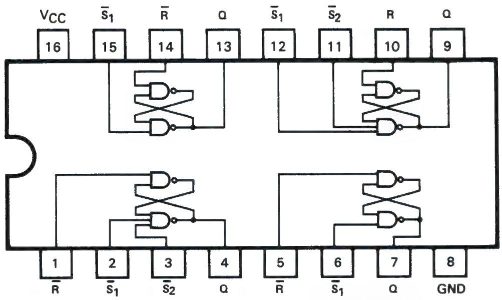
SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

F54LS/74LS279

QUAD SET-RESET LATCH



TRUTH TABLE

INPUTS			OUTPUT
$\bar{S}_1$	$\bar{S}_2$	$\bar{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS279XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS279XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			3.8	7.0	mA	V_{CC} = MAX	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 5-322 for Waveforms)

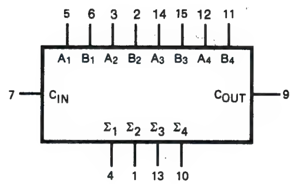
SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, $\bar{S}$ to Output			22 15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay, $\bar{R}$ to Output			27	ns	

F54LS/74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION — The 54LS/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 — A_4, B_1 — B_4) and a Carry Input (C_{IN}). It generates the binary Sum outputs (Σ_1 — Σ_4) and the Carry Output (C_{OUT}) from the most significant bit. The device operates with either active HIGH or active LOW operands (positive or negative logic). It is identical in function with 7483A and features corner power pins.

LOGIC SYMBOL



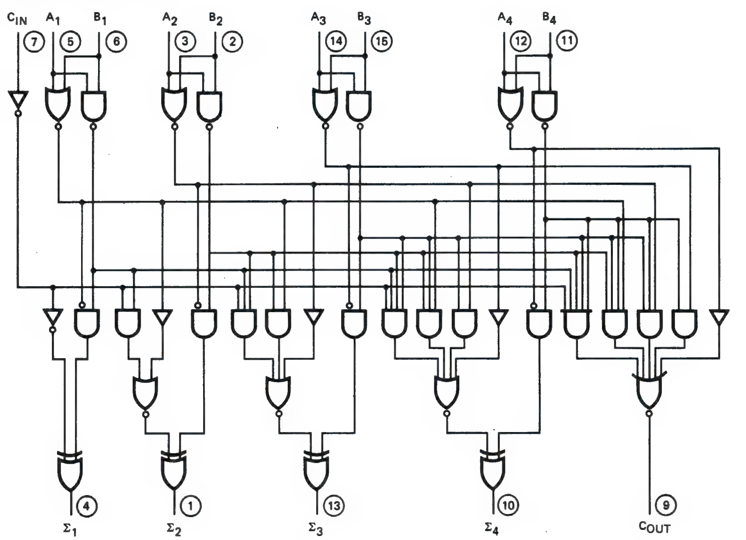
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

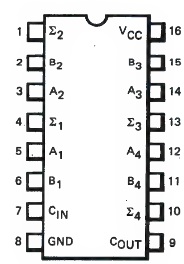
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION —This device adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 — Σ_4) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the device can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarity assigned to pins 7, 5 or 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS283XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS283XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs = 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output		14 13	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		17 19	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output		12 9	17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output		14 10	17 17	ns	

AC WAVEFORMS

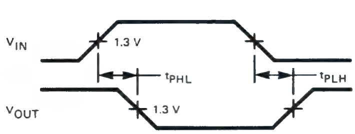


Fig. 1

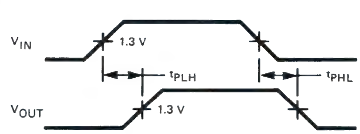


Fig. 2

5

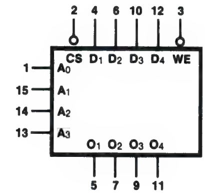
F54LS/74LS289

64-BIT RANDOM ACCESS MEMORY WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION — The 54LS/74LS289 is a high-speed, low-power 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- OPEN COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS
- BUFFERED INPUTS MINIMIZE LOADING
- ADDRESS DECODING ON-CHIP
- DIODE CLAMPED INPUTS MINIMIZE RINGING
- LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

A_n	Address Input
$\overline{CS}$	Chip Select (Active LOW) Input
D_n	Data Input
O_n	Data (Inverted) Output
$\overline{WE}$	Write Enable (Active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

F54LS/74LS290 • F54LS/74LS293

DECADE COUNTER   4-BIT BINARY COUNTER

DESCRIPTION—The 54LS/74LS290 and 54LS/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (54LS/74LS290) or divide-by-eight (54LS/74LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the 54LS/74LS290 also has a 2-input gated Master Set (Preset 9).

- **CORNER POWER PIN VERSIONS OF THE 54LS/74LS90 and 54LS/74LS93**
- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

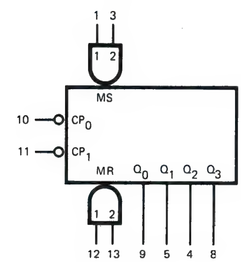
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷ Section.	3.0 U.L.	1.U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ Section (54LS/74LS290).	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 8 Section (54LS/74LS293).	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, 54LS/74LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

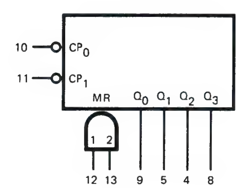
LOGIC SYMBOL

54LS/74LS290



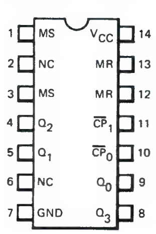
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

54LS/74LS293



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

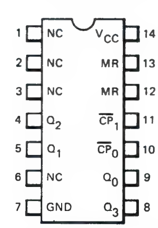
CONNECTION DIAGRAM **54LS/74LS290**
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC — No Internal Connection

CONNECTION DIAGRAM **54LS/74LS293**
DIP (TOP VIEW)

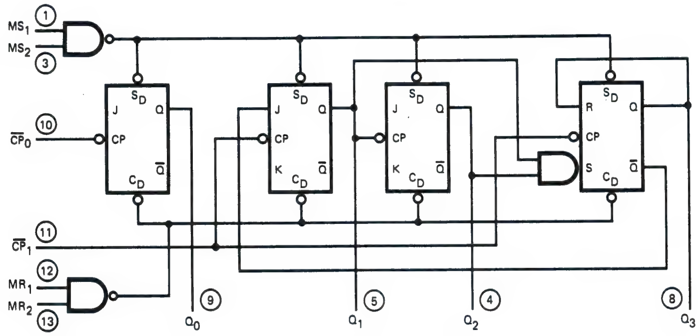


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC — No internal connection

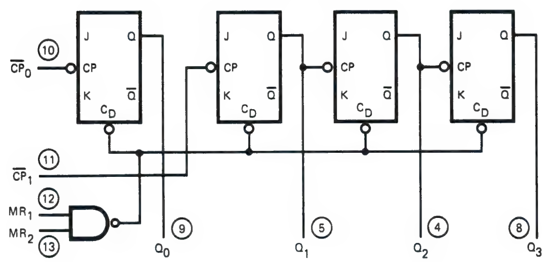
LOGIC DIAGRAMS

54LS/74LS290



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

54LS/74LS293



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

FUNCTIONAL DESCRIPTION—These devices are 4-bit ripple-type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (54LS/74LS290) or divide-by-eight (54LS/74LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the 54LS/74LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

54LS/74LS290

A. BCD Decade (8421) Counter — the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

54LS/74LS293

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

54LS/74LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

54LS/74LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

54LS/74LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

54LS/74LS293
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

5

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS290XM 54LS293XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS290XC 74LS293XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS290) $\overline{CP}_1$ (LS293)				 20 120 80 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	MS, MR $\overline{CP}_0$, $\overline{CP}_1$ (LS293) $\overline{CP}_1$ (LS290)				0.1 0.4 0.8	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS290) $\overline{CP}_1$ (LS293)				 −0.4 −2.4 −3.2 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS290 MIN	LIMITS 54LS/74LS290 MAX	LIMITS 54LS/74LS293 MIN	LIMITS 54LS/74LS293 MAX	UNITS	TEST CONDITIONS	
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		32 35	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		51 51	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		70 70	ns		
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30			ns	Fig. 3	
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40			ns	Fig. 2	
t_{PHL}	MR Input to Any Output		40		40	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS 54LS/74LS290 MIN	LIMITS 54LS/74LS290 MAX	LIMITS 54LS/74LS293 MIN	LIMITS 54LS/74LS293 MAX	UNITS	TEST CONDITIONS	
t_W	$\overline{CP}_0$ Pulse Width	15		15		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	30		30		ns		
t_W	MS Pulse Width	15				ns	Fig. 2, 3	
t_W	MR Pulse Width	15		15		ns	Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25				ns	Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		ns	Fig. 2	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

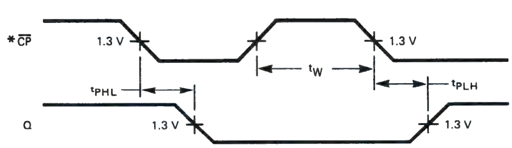


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

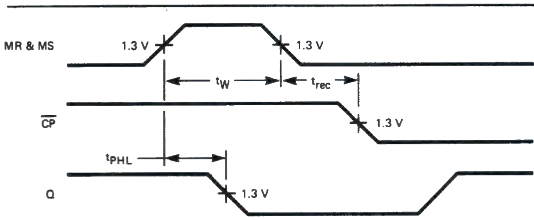


Fig. 2

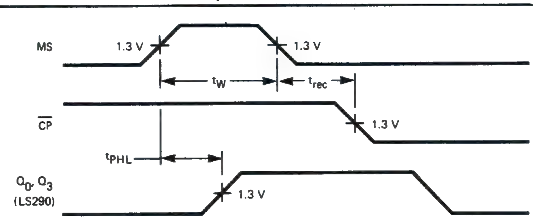


Fig. 3

F54LS/74LS295A

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

The 3-State output buffers are controlled by an active HIGH output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

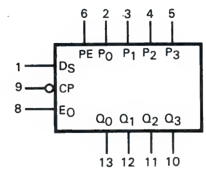
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Input	0.5 U.L.	0.25 U.L.
E_O	Output Enable Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Pulse (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	3-State Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

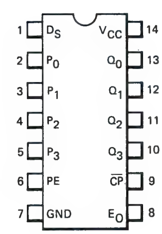
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



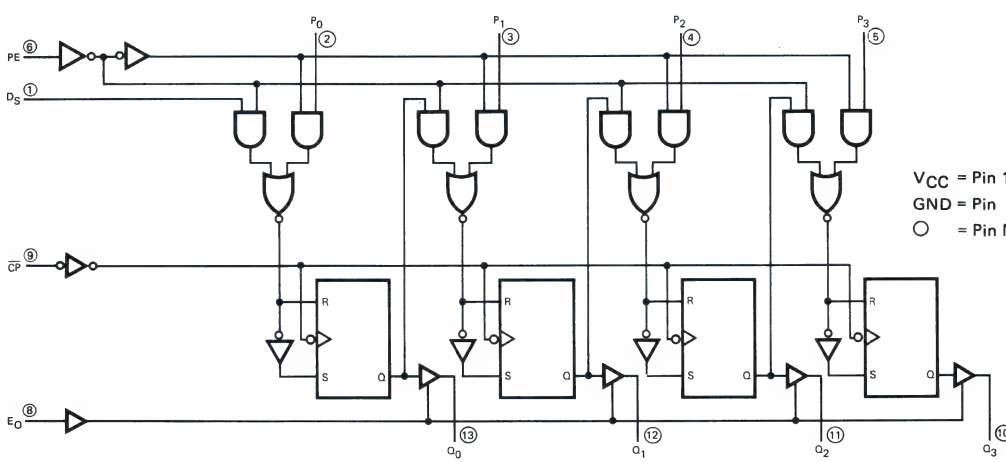
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — This device is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data ($P_0 - P_3$) inputs and four parallel 3-State output buffers ($Q_0 - Q_3$). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs ($P_0 - P_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edged-triggered and must be stable only one set-up time before the HIGH or LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (E_0). When the E_0 is HIGH, the four register outputs appear at the $Q_0 - Q_3$ outputs. When E_0 is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e., the input transitions on the E_0 input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	↓	l	X	L	q_0	q_1	q_2
	l	↓	h	X	H	q_0	q_1	q_2
Parallel Load	h	↓	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

L = LOW Voltage Levels
H = HIGH Voltage Levels
X = Immaterial
$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.
l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS295AXM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS295AXC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC	2.4	3.4			I_{OH} = −2.6 mA	V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off Current LOW				20	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH			14	23	mA	V_{CC} = MAX, V_{CP} = ⎍, V_E = 4.5 V	
	Power Supply Current, Outputs Off			15	25	mA	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Shift Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		24 16	30 26	ns	Fig. 1	C_L = 15 pF

AC CHARACTERISTICS: for 3-State Output Buffers (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		14	20	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		17	24	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		15	20	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	20	7		ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	20	7		ns	Fig. 1	
t_h(Data)	Hold Time, Data to Clock	10	2		ns	Fig. 1	
t_s(PE)	Set-up Time, PE to Clock	20	7		ns	Fig. 2	
t_h(PE)	Hold Time, PE to Clock	0			ns	Fig. 2	

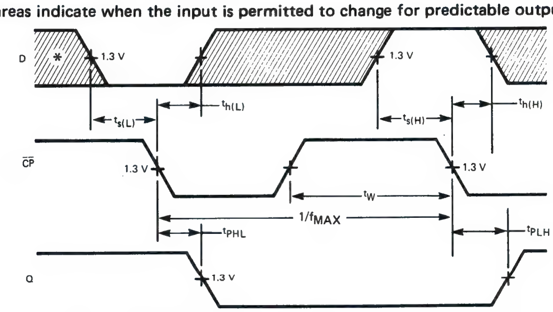
DEFINITION OF TERMS

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1

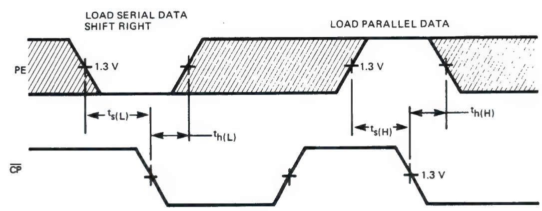


Fig. 2

F54LS/74LS298

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION—The 54LS/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

The device is fabricated with the Schottky barrier process for high speed and is completely compatible with all Fairchild TTL families.

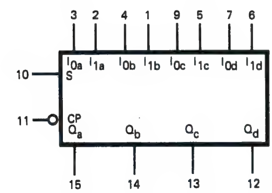
- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
$Q_a - Q_d$	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

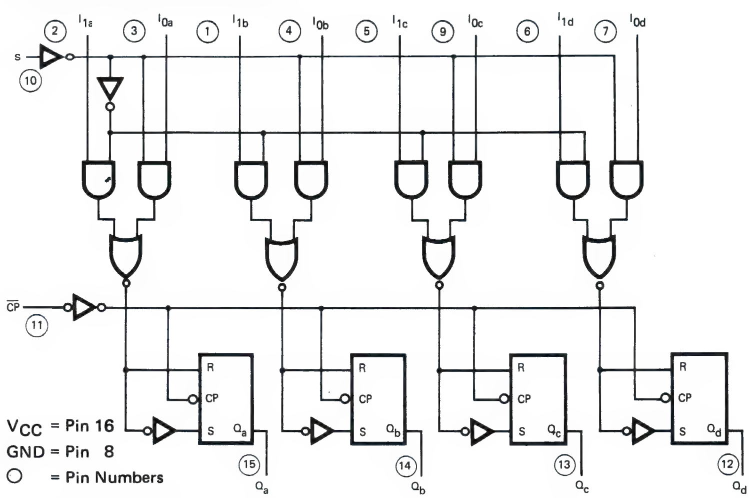
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL

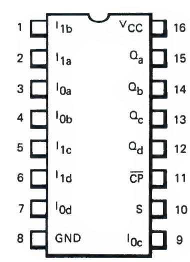


V_{CC} = Pin 16
GND = Pin 8

LOGIC OR BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — This device is a high-speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH-to-LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS298XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS298XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		19 16	25 25	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF

AC SET-UP REQUIREMENTS: T_A = 25°C

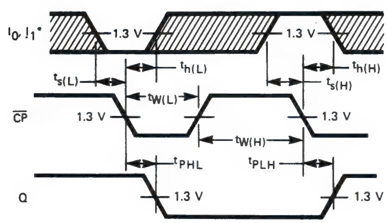
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20	11		ns	Fig. 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clock Pulse Width (LOW)	20	11		ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	15	10		ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	5.0	1		ns		
$t_{s(S)}$	Set-up Time, Select to Clock	25	20		ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0	-2		ns		

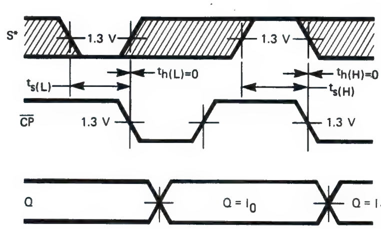
DEFINITION OF TERMS:

SET-UP TIME (t_s)—is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h)—is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

AC WAVEFORMS





*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1 **Fig. 2**

F54LS/74LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

DESCRIPTION — The 54LS/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

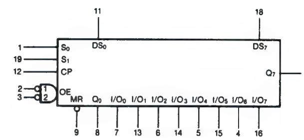
- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE**
- **SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	0.5 U.L.	0.25 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{MR}$	Asynchronous Master Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	0.5 U.L.

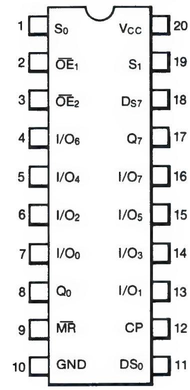
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.
c. The Output LOW drive factor is 7.5 U.L. for Military (XM) and 15 U.L. for Commercial (XC), the Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



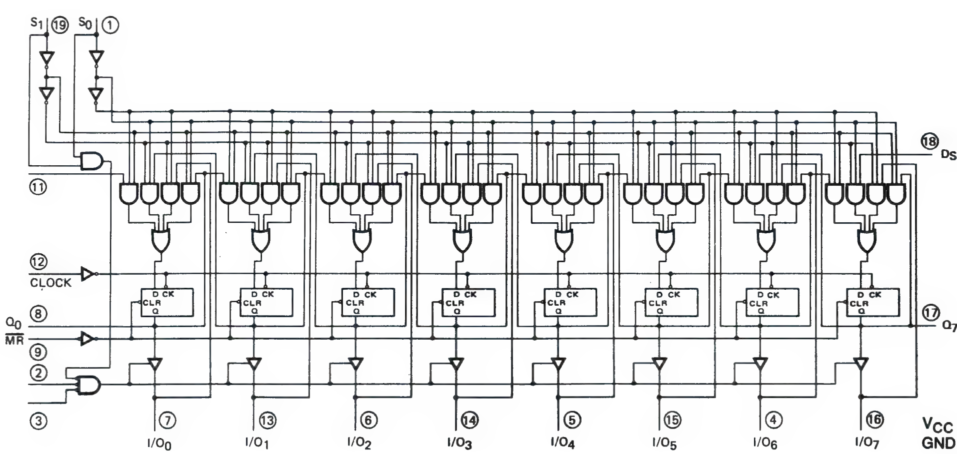
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
O = Pin Numbers

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-5.0 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS299XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS299XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage Q_0, Q_7	XM	2.4	3.4		V	I_{OH} = -400 µA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V		
V_{OH}	Output HIGH Voltage I/O_0 thru I/O_7	XM	2.4	3.4		V	I_{OH} = -1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = -2.6 mA	
V_{OL}	Output LOW Voltage Q_0, Q_7	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
V_{OL}	Output LOW Voltage I/O_0 thru I/O_7	XM,XC		0.25	0.4	V	I_{OL} = 12.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24.0 mA	
I_{OZH}	Output Off Current HIGH				40	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, $\overline{V_E}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				-400	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, $\overline{V_E}$ = 2.0 V	
I_{IH}	Input HIGH Current All inputs except S_0, S_1 S_0, S_1				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage All inputs except S_0, S_1 S_0, S_1				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current All inputs except S_0, S_1 S_0, S_1				-0.4 -0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)	I/O_0 thru I/O_7	-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
		Q_0, Q_7	-20		-100			
I_{CC}	Power Supply Current			35	60	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

FUNCTION TABLE

INPUTS								RESPONSE
$\overline{MR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
X	L	H	X	X	$\uparrow$	D	X	Shift Right; $D \rightarrow Q_0$; $Q_0 \rightarrow Q_1$; etc.
H	L	H	L	L	$\uparrow$	D	X	Shift Right; $D \rightarrow Q_0$ & I/O_0; $Q_0 \rightarrow Q_1$ & I/O_1; etc.
H	H	L	X	X	$\uparrow$	X	D	Shift Left; $D \rightarrow Q_7$; $Q_7 \rightarrow Q_6$; etc.
H	H	L	L	L	$\uparrow$	X	D	Shift Left; $D \rightarrow Q_7$ & I/O_7; $Q_7 \rightarrow Q_6$ & I/O_6; etc.
H	H	H	X	X	$\uparrow$	X	X	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wH (CP)	Minimum Clock Pulse Width HIGH	20			ns	
t_wL (CP)	Minimum Clock Pulse Width LOW	20			ns	
t_wL (MR)	Minimum Master Reset Pulse Width LOW	20			ns	
t_s	Set-up Time, S_0 or S_1 to CP	10			ns	
t_h	Hold Time, S_0 or S_1 to CP	10			ns	
t_s (H)	Set-up Time I/O_0 thru I/O_7, DS_0, DS_7 to CP (HIGH)	20			ns	
t_s (L)	Set-up Time I/O_0 thru I/O_7, DS_0, DS_7 to CP (LOW)	20			ns	
t_h	Hold Time (HIGH or LOW) I/O_0 thru I/O_7, DS_0, DS_7 to CP	0			ns	
t_{rec}	Master Reset Recovery Time	20			ns	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Input Frequency	35	50		MHz	$V_{CC} = 5.0$ V
t_{PHL} t_{PLH}	Propagation Delay, Clock To Q_0 or Q_7			25 25	ns	$C_L = 15$ pF
t_{PHL} t_{PLH}	Propagation Delay, Clock To I/O_0 thru I/O_7			25 25	ns	
t_{PHL} t_{PHL}	Master Reset To Q_0 or Q_7 Master Reset To I/O_0 thru I/O_7			35 35	ns	
t_{PZH} t_{PZL}	Output Enable Time			35 35	ns	$C_L = 5$ pF $R_L = 667\ \Omega$
t_{PHZ} t_{PLZ}	Output Disable Time			25 25	ns	$V_{CC} = 5.0$ V

F54LS/74LS323

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

DESCRIPTION—The 54LS/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the 54LS/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading.

Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

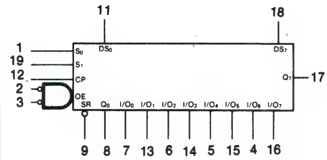
- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD AND STORE**
- **SEPARATE CONTINUOUS INPUTS AND OUTPUTS FROM Q_0 AND Q_7 ALLOW EASY CASCADING**
- **FULLY SYNCHRONOUS RESET**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input For Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input For Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	1.0 U.L.	0.5 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	
$\overline{SR}$	Synchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.

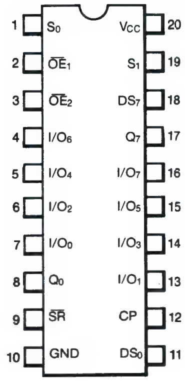
NOTES:
a. 1 TTL LOAD = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial Temperature Ranges.
c. The output LOW drive factor is 7.5 U.L. for Military (XM) and 15 U.L. for Commercial Temperature Ranges.
The output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL



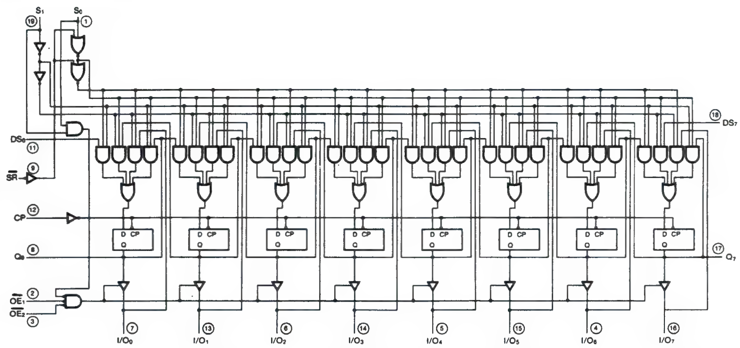
V_{CC} = 20
GND = 10

CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS323



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION The logic diagram and truth table indicate the functional characteristics of the 54LS/75LS323 Universal Shift/Storage Register. This device is similar in operation to the 54LS/74LS299 except for synchronous reset. A partial list of the common features are described below:

1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control (S_0, S_1) and data inputs (DS_0, DS_7, I/O_0-I/O_7) be stable at least a set-up time prior to the positive transition of the Clock Pulse.

2. When $S_0 = S_1 = 1$, I/O_0-I/O_7 are parallel inputs to flip-flops Q_0-Q_7 respectively, and the outputs of Q_0-Q_7 are in the high impedence state regardless of the state of $\overline{OE}_1$ or $\overline{OE}_2$.

An important unique feature of the 54LS/74LS323 is a fully Synchronous Reset that requires only to be stable at least one set-up time prior to the positive transition of the Clock Pulse.

TRUTH TABLE

INPUTS								RESPONSE
$\overline{SR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	↑	X	X	Synchronous Reset; $Q_0 = Q_7$ = LOW I/O voltage undetermined
L	X	X	X	H	↑	X	X	
L	H	H	X	X	↑	X	X	
L	L	X	L	L	↑	X	X	Synchronous Reset; $Q_0 = Q_7$ = LOW
L	X	L	L	L	↑	X	X	I/O voltage LOW
H	L	H	X	X	↑	D	X	Shift Right; D→Q_0; Q_0→Q_1; etc.
H	L	H	L	L	↑	D	X	Shift Right; D→Q_0 & I/O_0; Q_0→Q_1 & I/O_1; etc.
H	H	L	X	X	↑	X	D	Shift Left; D→Q_7; Q_7→Q_6; etc.
H	H	L	L	L	↑	X	D	Shift Left; D→Q_7 & I/O_7; Q_7→Q_6 & I/O_6; etc.
H	H	H	X	X	↑	X	X	Parallel Load I/O_n→Q_n
H	L	L	H	X	X	X	X	Hold; I/O Voltage Undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold; $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
VCC Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS323XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS323XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum input frequency	35	50		MHz	$V_{CC} = 5.0$ V
t_{PHL} t_{PLH}	Propagation Delay, CP To Q_0 or Q_7			25 25	ns	$C_L = 15$ pF
t_{PLH} t_{PLH}	Propagation Delay, CP To I/O_0 thru I/O_7			25 25	ns	
t_{PZH} t_{PZL}	Output Enable Time			35 35	ns	$C_L = 5$ pF $R_L = 665\ \Omega$
t_{PHZ} t_{PLZ}	Output Disable Time			25 25	ns	$V_{CC} = 5.0$ V

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wH (CP)	Minimum Clock Pulse Width HIGH	20			ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_wL (CP)	Minimum Clock Pulse Width LOW	20			ns	
t_s	Set-up Time, $\overline{SR}$ to CP	10			ns	
t_s	Set-up Time, S_0 or S to CP	10			ns	
t_h	Hold Time, $\overline{SR}$ to CP	10			ns	
t_h	Hold Time, S_0 or S to CP	10			ns	
t_s (H)	Set-up Time I/O_0 thru I/O_7, DS_0-DS_7 to CP (HIGH)	20			ns	
t_s (L)	Set-up Time I/O_0 thru I/O_7, DS_0-DS_7 to CP (LOW)	20			ns	
t_h	Hold Time (HIGH or LOW) I/O_0 thru I/O_7, DS_0-DS_7 to CP	0			ns	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

F54LS/74LS352

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The 54LS/74LS352 is a very high-speed Dual 4-Input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 54LS/74LS352 is the functional equivalent of the 54LS/74LS153 except with inverted outputs.

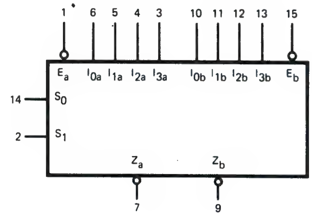
- **INVERTED VERSION OF THE 54LS/74LS153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.75 U.L.
$\overline{Z}$	Multiplexer Outputs (note b)	10 U.L.	5 (2.5) U.L.

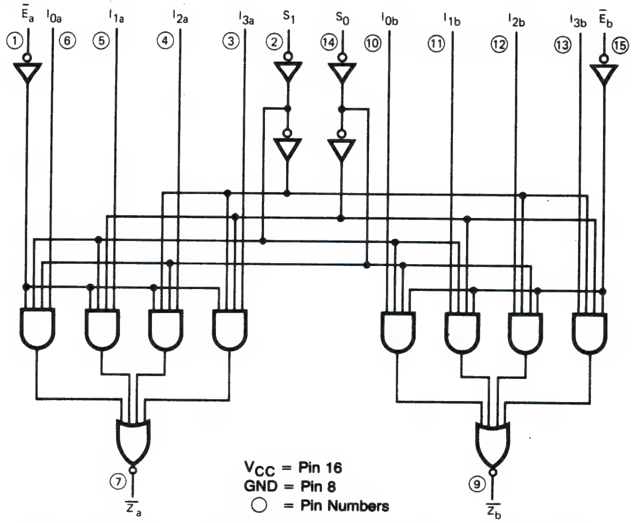
NOTES:
a. 1 TTL Unit Load (U.L.) = 40µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



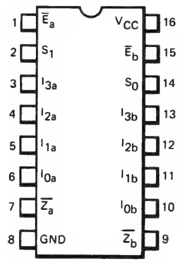
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 54LS/74LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{E}_a \cdot \overline{(I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)}$$
$$\overline{Z}_b = \overline{E}_b \cdot \overline{(I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)}$$

The 54LS/74LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The 54LS/74LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS352XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS352XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA	
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		16 17	25 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		11 15	18 22	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8 7	15 15	ns	Fig. 2	

AC WAVEFORMS

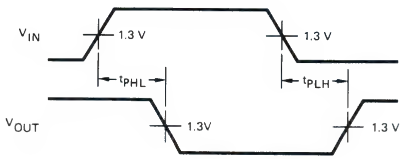


Fig. 1

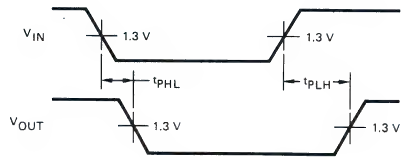


Fig. 2

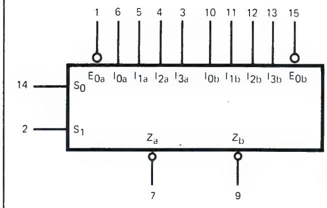
F54LS/74LS353

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The LSTTL/MSI 54LS/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{E}_0$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **INVERTED VERSION OF 54LS/74LS253**
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



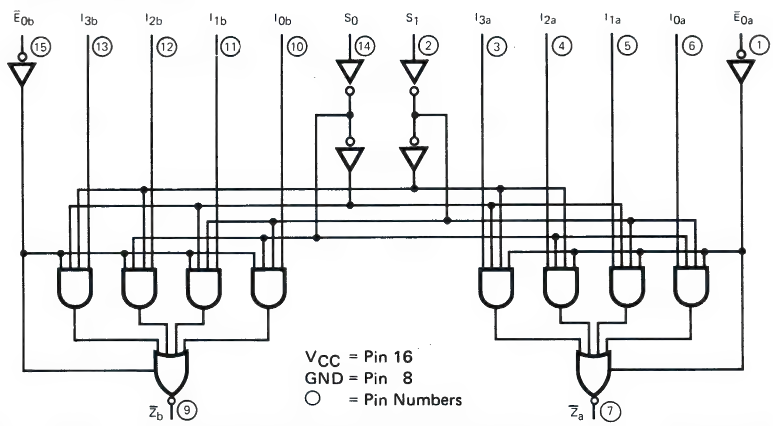
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

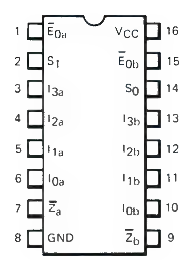
PIN NAMES		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_a$	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_b$	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 54LS/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The logic equations for the outputs are shown below:

$$\overline{Z_a} = \overline{\overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)}$$
$$\overline{Z_b} = \overline{\overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS353XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS353XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	29 24	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	18	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	32	ns	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	18	ns	Figs. 4, 5	

3-STATE WAVEFORMS

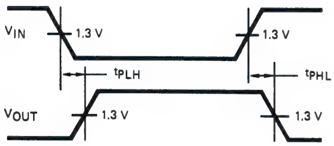


Fig. 1

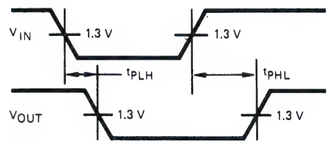


Fig. 2

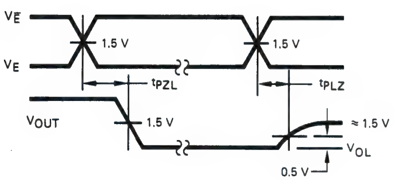


Fig. 3

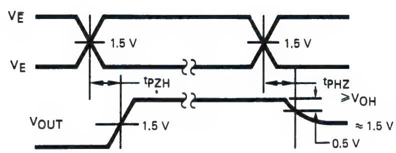
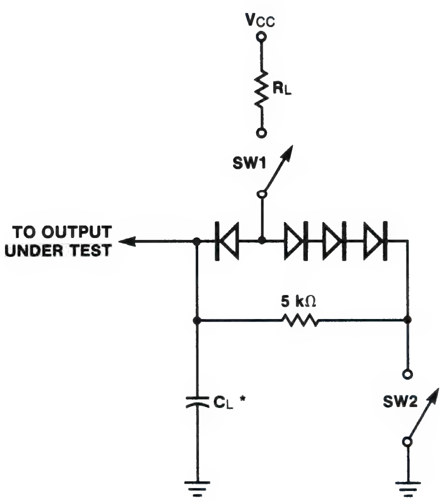


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance

Fig. 5

SWITCH POSITIONS

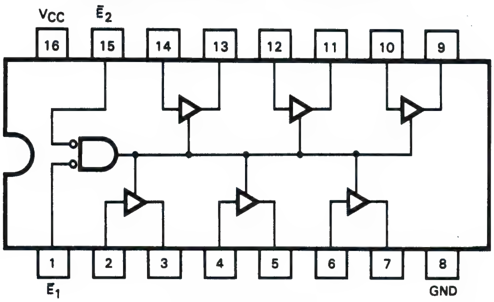
SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

F54LS/74LS365 • F54LS/74LS366
F54LS/74LS367 • F54LS/74LS368
3-STATE HEX BUFFERS

DESCRIPTION—These devices are high-speed Hex Buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

When the output Enable Input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

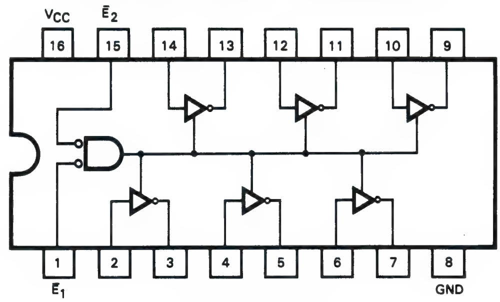
54LS/74LS365
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

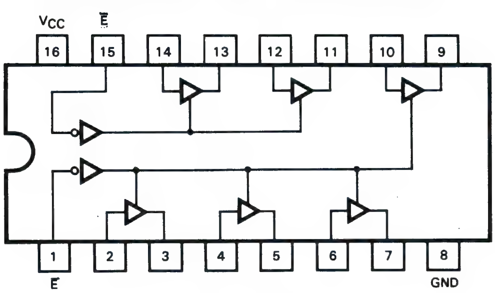
54LS/74LS366
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

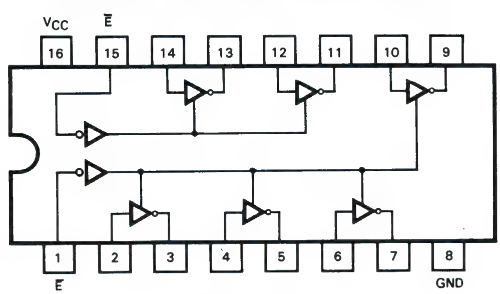
54LS/74LS367
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

54LS/74LS368
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS365XM 54LS366XM 54LS367XM 54LS368XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS365XC 74LS366XC 74LS367XC 74LS368XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		-40		-225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	54LS/74LS365/367		13.5	24	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	
		54LS/74LS366/368		11.8	21			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-322 for Waveforms)

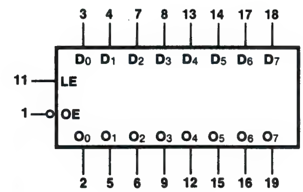
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS365/367			10 16	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS366/368			10 16	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 667 Ω

F54LS/74LS373
OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedence state.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**
- **HYSTERESIS ON LATCH ENABLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

LOGIC SYMBOL



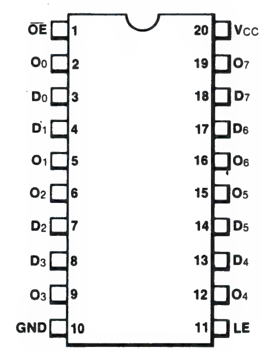
V_{CC} = Pin 20
GND = Pin10

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

CONNECTION DIAGRAM
DIP (TOP VIEW)



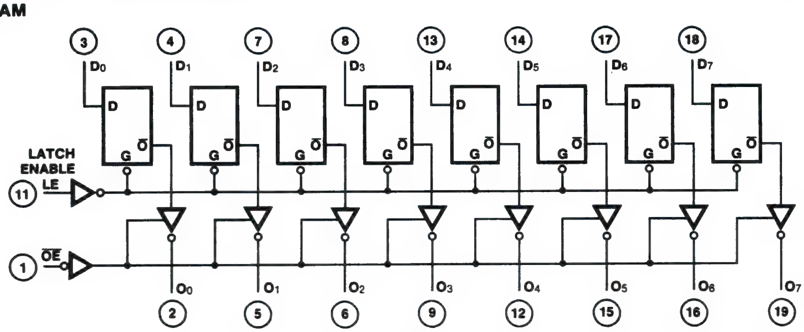
PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0 - D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) input	0.5 U.L.	0.25 U.L.
O_0 - O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

b) The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
○= Pin Numbers

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS373XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS373XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−20			mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs OFF			24	40	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_sD	Set-up Time Data to Negative Going LE	0	−2.0		ns	Fig. 1	
t_hD	Hold Time Data to Negative Going LE	10	7.0		ns	Fig. 1	V_{CC} = 5.0 V
t_wLE	Minimum LE Pulse Width HIGH or LOW	15	10		ns	Fig. 1	

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

AC CHARACTERISTICS : $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 16	18 27	ns	Fig. 1	$C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, LE to Output		14 24	25 36	ns	Fig. 1	$C_L = 15$ pF
t_{PZH}	Output Enable Time to HIGH Level		15	28	ns	Figs. 3, 4	$C_L = 15$ pF
t_{PZL}	Output Enable Time to LOW Level		22	36	ns	Figs. 2, 4	$R_L = 2.0$ kΩ
t_{PLZ}	Output Disable Time from LOW Level		13	25	ns	Figs. 2, 4	$C_L = 5.0$ pF
t_{PHZ}	Output Disable Time from HIGH Level		11	20	ns	Figs. 3, 4	$R_L = 2.0$ kΩ

AC WAVEFORMS

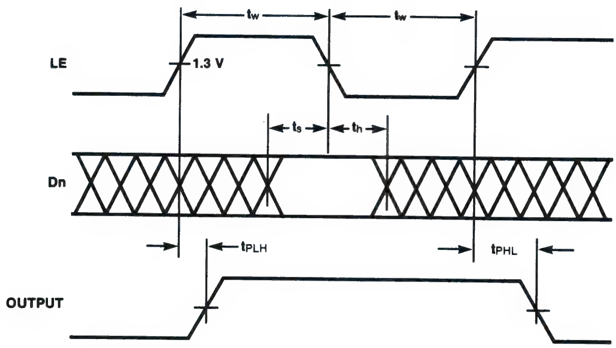


Fig. 1

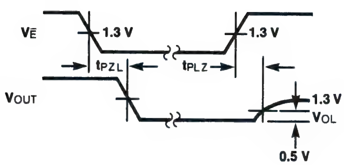


Fig. 2

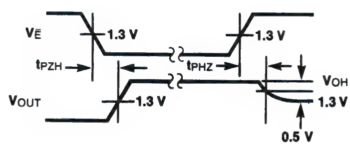
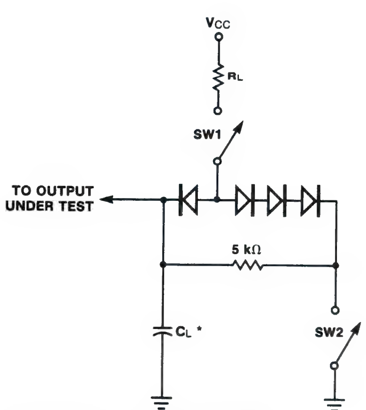


Fig. 3

AC LOAD CIRCUIT



*Includes Jip and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 4

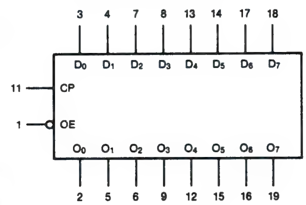
F54LS/74LS374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

DESCRIPTION—The 54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) is common to all flip-flops. The 54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Fairchild TTL families.

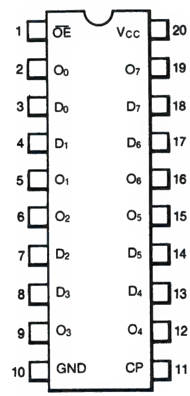
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **HYSTERISIS ON OUTPUT ENABLE INPUT TO IMPROVE NOISE MARGIN**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

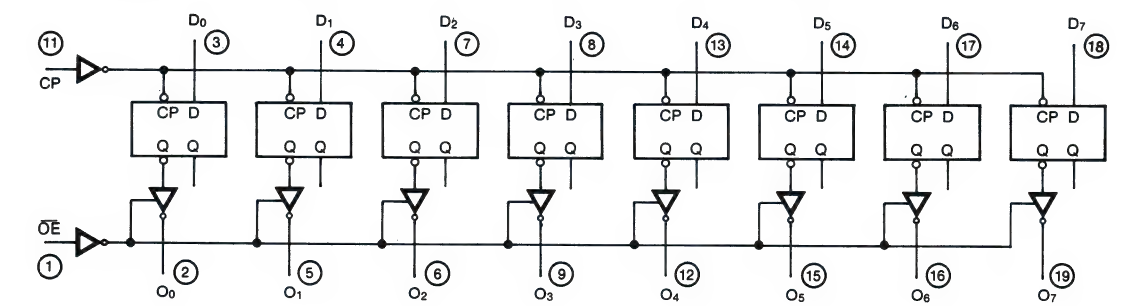


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0-O_7	Outputs (Note b)	65(25) U.L.	15(7.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 7.5 U.L. for military (XM) and 25 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



TRUTH TABLE

Dn	CP	$\overline{OE}$	On
H	↑	L	H
L	↑	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedence

*Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$)

FUNCTIONAL DESCRIPTION—The 54LS/74LS374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The Clock and Output Enable are common. The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are refected on the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedence state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 24 mA	V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
Icc	Power Supply Current, Outputs OFF			27	45	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0 V$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, CP To Output			28 34	ns	Fig. 1	$C_L = 15 pF$
t_{PZH}	Output Enable Time to HIGH Level			28	ns	Figs. 3, 4	$C_L = 15 pF$
t_{PZL}	Output Enable Time to LOW Level			36	ns	Figs. 2, 4	$R_L = 2 k\Omega$
t_{PLZ}	Output Disable Time from LOW Level			24	ns	Figs. 2, 4	$C_L = 5.0 pF$
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 3, 4	$R_L = 2 k\Omega$
f_{MAX}	Maximum Input Frequency	35	50		MHz	Fig. 1	$C_L = 45 pF$

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
T_wCP	Minimum Clock Pulse Width, HIGH or LOW	13	10		ns	Fig. 1	$V_{CC} = 5.0 V$
t_s	Minimum Set-up Time, Data to CP	20	15		ns	Fig. 1	
t_h	Minimum Hold Time, Data to CP	0	−3		ns	Fig. 1	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

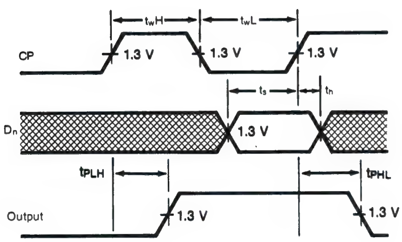


Fig. 1

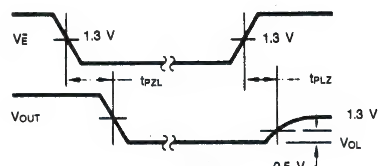


Fig. 2

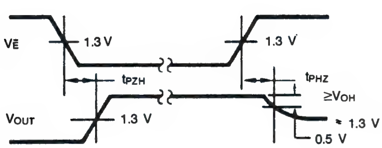
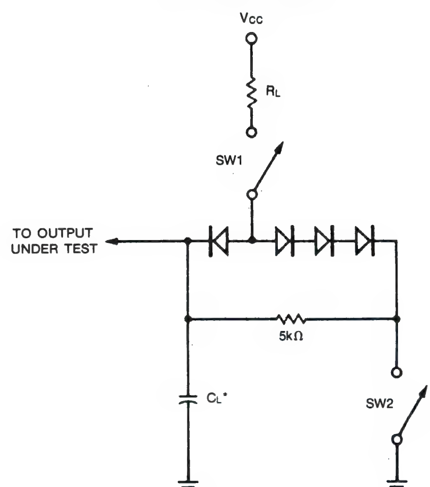


Fig. 3

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

Fig. 4

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

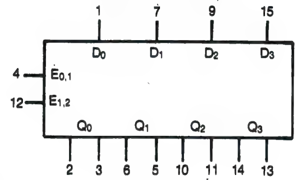
F54LS/74LS375

4-BIT LATCH

DESCRIPTION — The 54LS/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) input is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its set up time will be retained at the Q outputs.

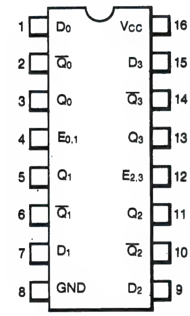
This device is functionally identical to the 54LS/74LS75 except for the corner power pins. For complete discussion of electrical characteristics, truth tables and operations information, refer to the 54LS/74LS75 data sheet.

LOGIC SYMBOL



V_{CC} = 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

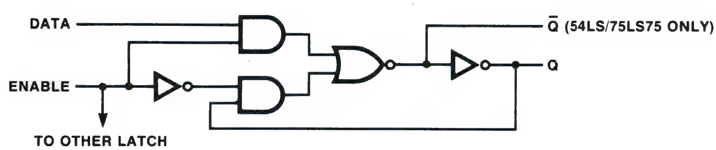
PIN NAMES

LOADING (Note a)

		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1-Q_4	Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_1$-$\overline{Q}_4$	Complementary Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



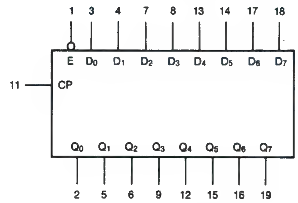
F54LS/74LS377

OCTAL D FLIP-FLOP WITH COMMON ENABLE AND CLOCK

DESCRIPTION: The 54LS/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

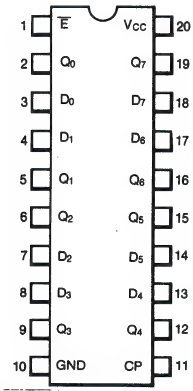
- **8-BIT HIGH SPEED PARALLEL REGISTERS**
- **POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



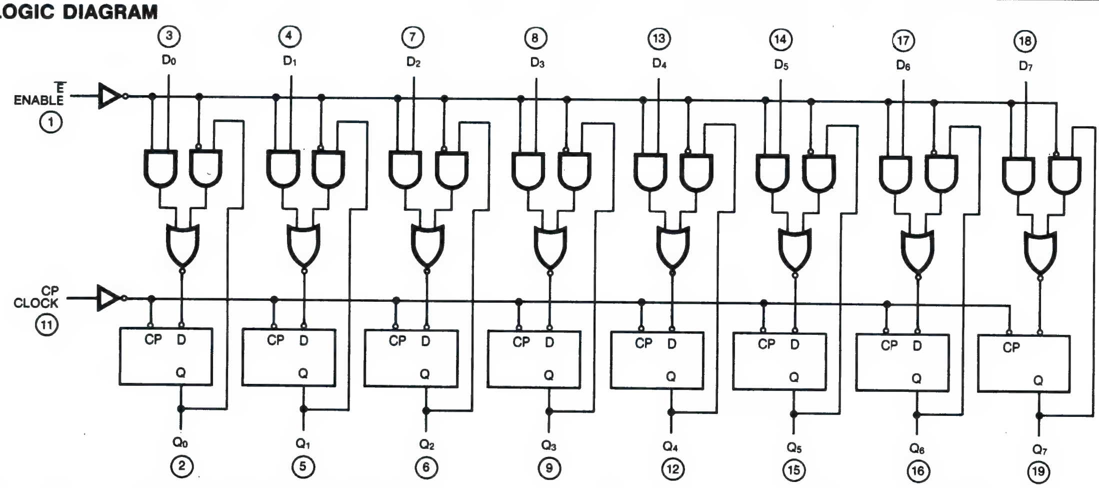
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_7	True Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION—The F54LS/74LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of (CP). When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	⨍	X	No Change
L	⨍	H	H
L	⨍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired.

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to + 15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage applied to outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS377XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS377XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage, All inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage, All inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = 18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.5		V	V_{CC} = MIN, I_{OH} = -400 μA	
		XC	2.7	3.5			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		XC		0.35	0.5		I_{OL} = 8 mA	or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			17	28	mA	V_{CC} = MAX	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under “worst case” conditions.
3. The specified LIMITS represent the “worst case” value for the parameter. Since these “worst case” values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25° C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
F_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0\ V$
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 18	27 27		Fig. 1	$C_L = 15\ pF$ $R_L = 2\ k\Omega$

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_w CP	Minimum Clockpulse Width	20			ns	Fig. 1	
t_s	Set-up Time Data to Clock (HIGH or LOW)	20			ns	Fig. 1	
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1	
$t_s(H)$	Set-up Time HIGH, Enable to Clock	10			ns	Fig. 1	$V_{CC} = 5.0\ V$
$t_h(H)$	Hold Time HIGH, Enable to Clock	5			ns	Fig. 1	CL = 15pF
$t_s(L)$	Set-up Time LOW, Enable to Clock	25			ns	Fig. 1	RL = 2kΩ
$t_h(L)$	Hold Time LOW, Enable to Clock	5			ns	Fig. 1	

DEFINITION OF TERMS:

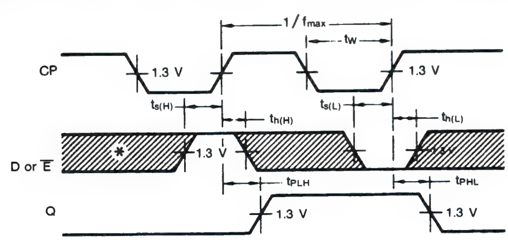
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA OR ENABLE TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

F54LS/74LS378

HEX PARALLEL D REGISTER WITH ENABLE

DESCRIPTION – The 54LS/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the 54LS/74LS174, but with common Enable rather than common Master Reset.

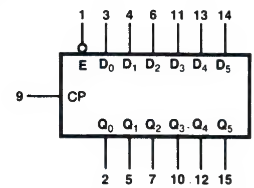
- **6-BIT HIGH-SPEED PARALLEL REGISTER**
- **POSITIVE EDGE-TRIGGERED D-TYPE INPUTS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULL TTL AND CMOS COMPATIBLE**

PIN NAMES / **LOADING** (Note a)

		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_5	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge Input)	0.5 U.L.	0.25 U.L.
Q_0-Q_5	True Outputs (Note b)	0.10 U.L.	0.25 U.L.

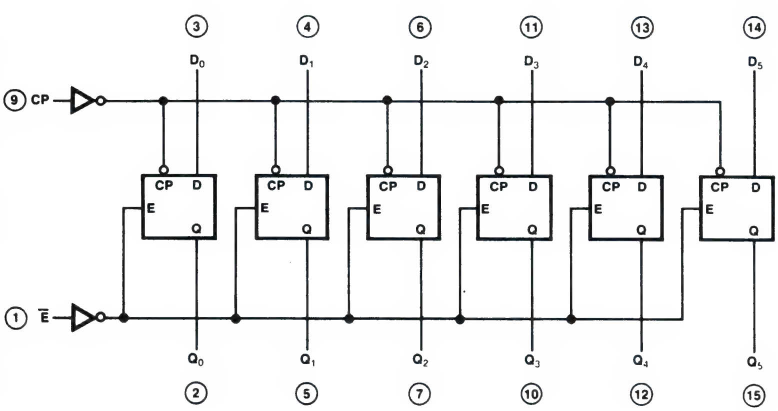
Notes:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH 1.6mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL

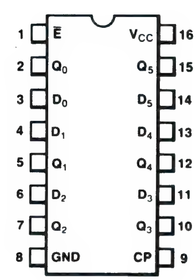


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 54LS/74LS378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip flops.

When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	⎍	X	No change
L	⎍	H	H
L	⎍	L	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS/74LS378XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
54LS/74LS378XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current (Note 6)			16	27	mA	V_{CC} = MAX	

5

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

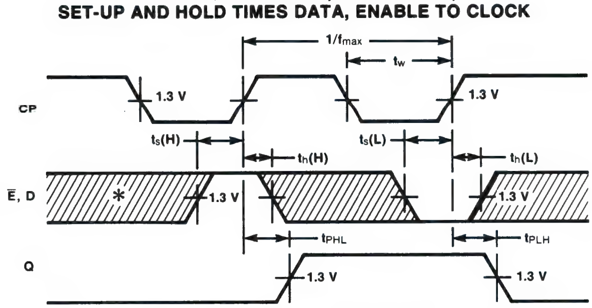
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	CP to Q Output			27 27	ns ns	Fig. 1	V_{CC} = 5.0 V
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1	V_{CC} = 5.0 V
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1.	
t_s	Set-up Time, Enable to Clock (HIGH or LOW)	30			ns	Fig. 1	
t_h	Hold Time Enable to Clock (HIGH or LOW)	5			ns	Fig. 1	
t_{WCP}	Minimum Clock Pulse Width	20					

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA, ENABLE TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

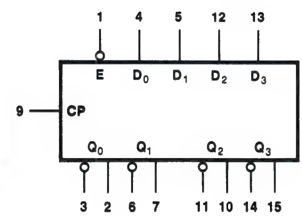
F54LS/74LS379

QUAD PARALLEL REGISTER WITH ENABLE

DESCRIPTION — The F54LS/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the 54LS/74LS175 but features the common Enable rather than common Master Reset.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	True Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_0$-$\overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5 (2.5) U.L.

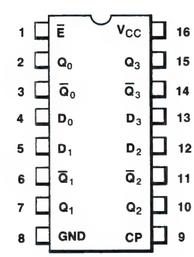
Notes:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

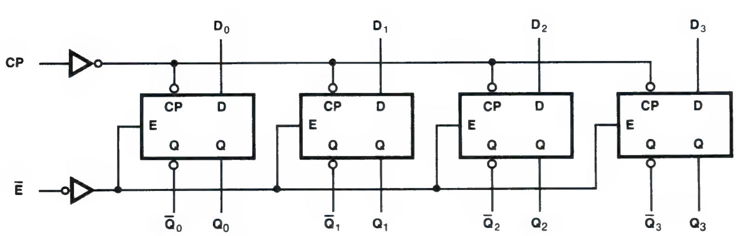
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The 54LS/74LS379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	No Change	No Change
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS379XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS379XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current $\overline{E}$, D_0-D_3,CP				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input HIGH Current at MAX Input Voltage $\overline{E}$, D_0-D_3, CP				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current $\overline{E}$, D_0-D_3, CP				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				18	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

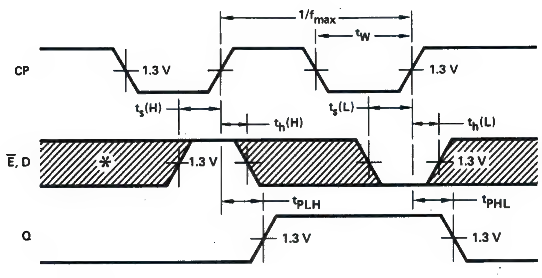
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	CP to Output			20 22	ns	Fig. 1, $V_{CC} = 5.0V$ $C_L = 15$ pF
f_{MAX}	Maximum Clock Frequency	30	45		MHz	

AC SET-UP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_s	Set-Up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1
t_s	Set-up Time, Enable to Clock	30			ns	Fig. 1
t_h	Hold Time, Enable to Clock	5			ns	Fig. 1
t_wCP	Minimum Clock Pulse Width	17	10		ns	

AC WAVEFORMS

**CLOCK TO OUTPUT DELAYS,
CLOCK PULSE WIDTH, FREQUENCY,
SET-UP AND HOLD TIMES DATA, ENABLE TO CLOCK**



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

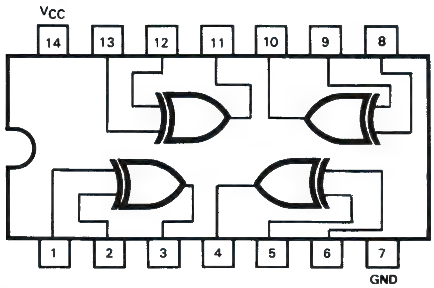
HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

5

F54LS/74LS386

QUAD 2-INPUT EXCLUSIVE-OR GATE

CONNECTION AND LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
54LS386XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS386XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_C = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Supply Current			6.1	10	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 5-322 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

F54LS/74LS390 • F54LS/74LS393

DUAL DECADE COUNTER
DUAL 4-STAGE BINARY COUNTER

DESCRIPTION — The 54LS/74LS390 and 54LS/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a bi-quinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the 'LS390 and the 'LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

FEATURES

- **DUAL VERSIONS OF LS290 AND LS293**
- **LS390 HAS SEPARATE CLOCKS ALLOWING ÷2, ÷2.5, ÷5**
- **INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER**
- **TYPICAL MAX COUNT FREQUENCY OF 50 MHZ**
- **INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}$	Clock (Active LOW going edge) Input to ÷16 (LS393)	0.5 U.L.	1.0 U.L.
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Flip-Flop outputs (Note b)	10 U.L.	5(2.5) U.L.

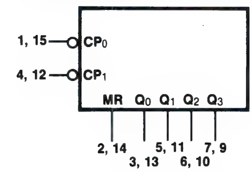
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FUNCTIONAL DESCRIPTION — Each half of the 54LS/74LS393 Operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the 'LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 4.2.1 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $\overline{CP}_1$ and connect the Q_3 output to the $\overline{CP}_0$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{CP}_0$ and the Q_0 output is connected to $\overline{CP}_1$, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of 'LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

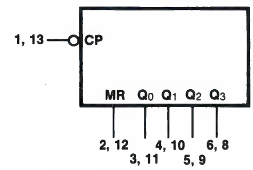
LOGIC SYMBOLS

54LS/74LS390 One Half Shown



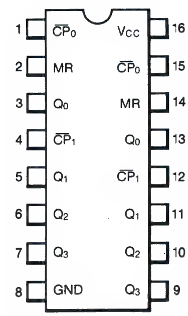
V_{CC} = Pin 16
GND = Pin 8

54LS/74LS393 One Half Shown

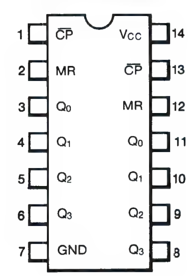


CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/74LS390

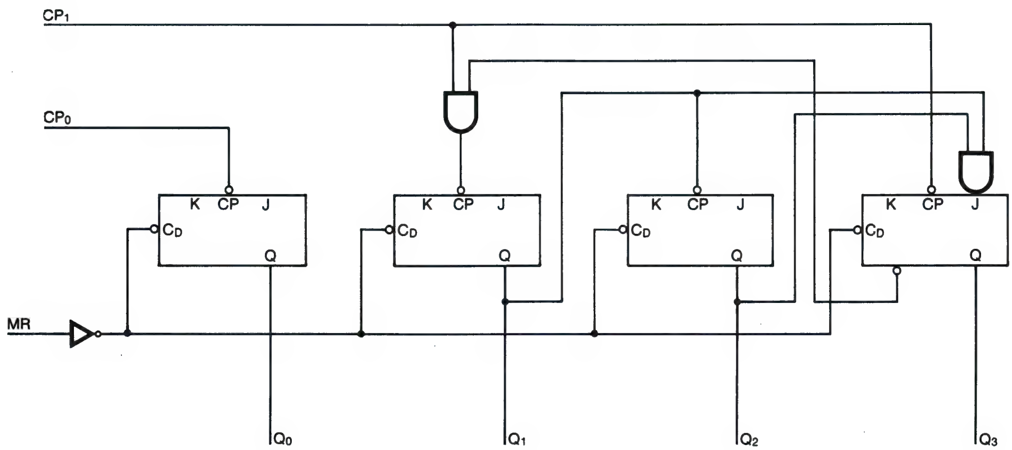


54LS/74LS393

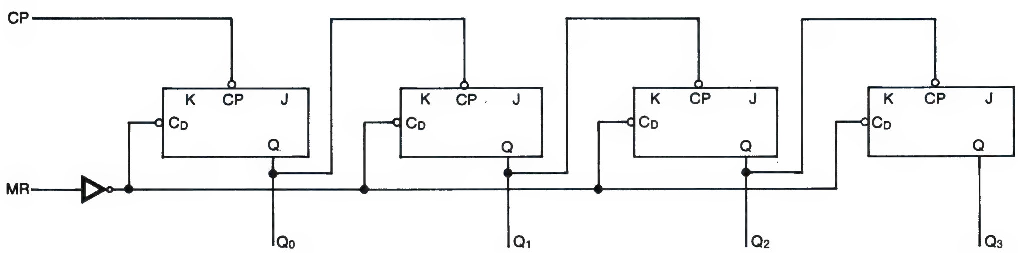


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

54LS/74LS390 LOGIC DIAGRAM (one half shown)



54LS/74LS393 LOGIC DIAGRAM (one half shown)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° to +125°C
Temperature (Ambient) Under Bias	-55° to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Curent (dc)	+30 mA to +5.0 mA
Voltage Applied to Outputs (Outputs HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS390XM 54LS393XM	4.5 V	5.0 V	5.5 V	-55°C to +125°C
74LS390XC 74LS393XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

54LS/74LS390 BCD TRUTH TABLE (Input on $\overline{CP}_0$; Q_0 $\overline{CP}_1$)

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

54LS/74LS390 ÷ 5 TRUTH TABLE (Input on $\overline{CP}_1$)

COUNT	OUTPUTS Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

54LS/74LS393 TRUTH TABLE

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMTER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 μA V_{IN} = V_{IL} or V_{IH} per Truth Table
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 8 mA; V_{CC} = MIN V_{IH} or
		XC		0.35	0.5		I_{OL} = 8 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{CP}$, $\overline{CP}_0$, $\overline{CP}_1$ MR				20	μA	V_{CC} = MAX V_{IN} = 2.7 V
I_{IL}	Input LOW Current MR $\overline{CP}$, $\overline{CP}_0$ $\overline{CP}_1$				 -0.4 -1.6 -2.4	mA	V_{CC} = MAX V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		-20		-100	mA	V_{CC} = MAX V_{OUT} = 0 V
I_{CC}	Power Supply Current	54LS/74LS393		20	25	mA	V_{CC} = MAX
				20	26		

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC2} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one outut should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	$\overline{CP}$ or $\overline{CP}_0$ to Q_0		10 10	15 15	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_1		23 23	30 30	ns	Fig. 1	
t_{PHL}	MR to Any Q		30	35	ns	Fig. 2	
f_{MAX}	$\overline{CP}$ or $\overline{CP}_0$ Input Count Frequency	40	50		MHz	Fig. 1	
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	20	25		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W	$\overline{CP}$ or $\overline{CP}_0$ Pulse Width	12	9		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	24	20		ns	Fig. 1	
t_W	MR Pulse Width	18	15		ns	Fig. 2	
t_{rec}	MR to $\overline{CP}$	15	10		ns	Fig. 2	

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

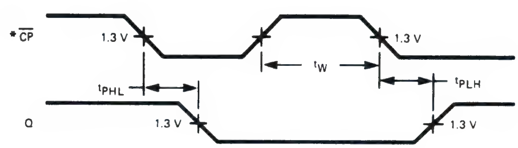


Fig. 1

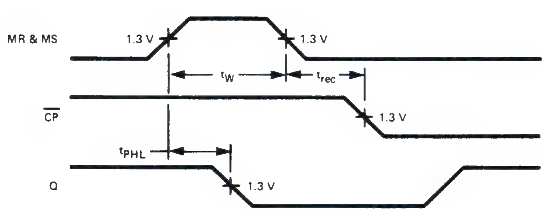


Fig. 2

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

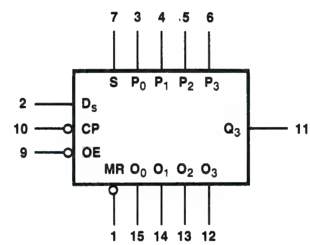
F54LS/74LS395

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active LOW Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- **SHIFT LEFT OR PARALLEL 4-BIT REGISTER**
- **3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

LOGIC SYMBOL



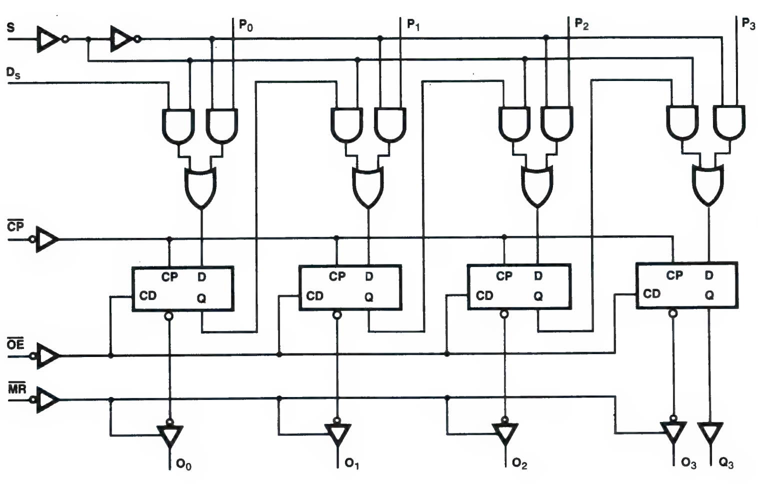
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES / **LOADING** (Note a)

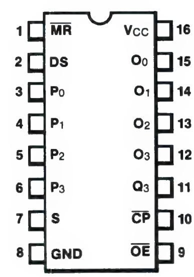
		HIGH	LOW
P_0-P_3	Parallel inputs	0.5 U.L.	0.25 U.L.
D_S	Serial Data input	0.5 U.L.	0.25 U.L.
S	Mode Select input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW) input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) input	0.5 U.L.	0.25 U.L.
O_0-O_3	3-State Register Outputs	10 U.L.	5 (2.5) U.L.
Q_3	Register Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS/74LS395XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
54LS/74LS395XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 54LS/74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (Pn) input or from the preceding stage. When the Select input is HIGH, the Pn inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_s and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1, and O_1 to P_0, with P_3 acting as the linking input from another package.

When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the O_0-O_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4			V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4				I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM, XC			0.4	V	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC			0.5	V	I_{OL} = 8.0mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX. V_{OUT} = 0.5 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX. V_{IN} = 2.7 V	
					100	μA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Outputs HIGH				29	mA	V_{CC} = MAX. V_{CP} = ⎍, V_E = 4.5 V	
	Power Supply Current Outputs LOW				25		V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V	

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Shift Frequency	30			MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Propagation Delay, Clock to Output			35	ns	Fig. 1	
t_{PHL}				25			
t_{PHL}	Propagation Delay MR to Output			35	ns	Fig. 1	

AC CHARACTERISTICS: For 3-State Output Buffers

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PZH}	Output Enable Time to HIGH Level			20	ns	Fig. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			20	ns	Fig. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			17	ns	Fig. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 2 kΩ

5

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_wCP	Clock Pulse Width	18			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s	Set-up Time, Data to Clock	20			ns	Fig. 1	
t_h	Hold Time, Data to Clock	5			ns	Fig. 1	
t_s	Set-up Time, Select to Clock	20			ns	Fig. 2	
t_h	Hold Time, Select to Clock	5			ns	Fig. 2	
t_wMR	Master Reset Minimum Pulse Width	20			ns	Fig. 1	

MODE SELECT — TRUTH TABLE

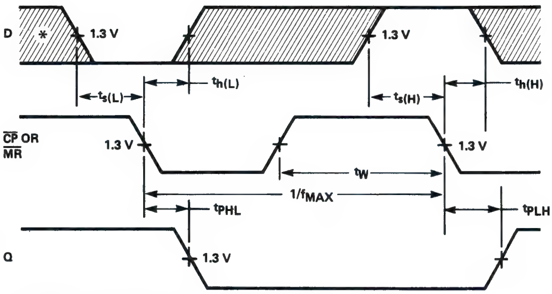
Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_s	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	↓	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	↓	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	↓	H	X	P_n	P_0	P_1	P_2	P_3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
$t_{n, n+1}$ = time before and after CP HIGH-to-LOW transition

NOTE:
When $\overline{OE}$ is LOW, outputs O_0-O_3 are in the high impedance state; however, this does not affect other operations or the Q_3 output.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for S = LOW and P_n for S = HIGH.

Fig. 1

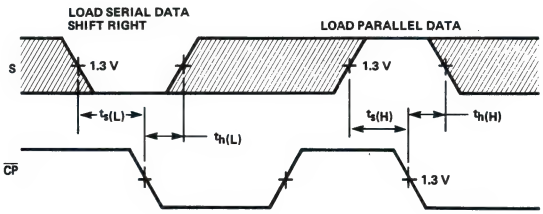


Fig. 2

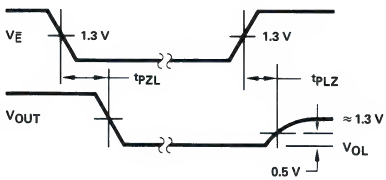


Fig. 3

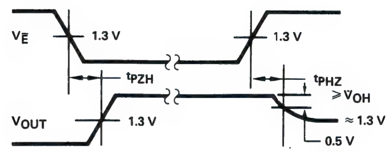
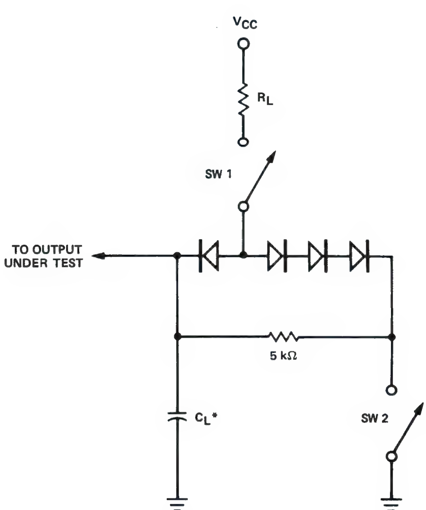


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

F54LS/74LS398 • F54LS/74LS399

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION—The 54LS/74LS398 and 54LS/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The 54LS/74LS398 features both Q and $\overline{Q}$ inputs, while the 54LS/74LS399 has only Q outputs.

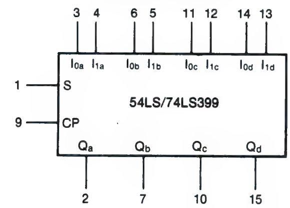
- **SELECT FROM TWO DATA SOURCES**
- **FULLY POSITIVE EDGE-TRIGGERED OPERATION**
- **BOTH TRUE AND COMPLEMENTED OUTPUTS ON 54LS/74LS398**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
I_{0a} — I_{0d}	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
I_{1a} — I_{0d}	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q_a — Q_d	Register True Outputs (Note b)	1.0 U.L.	5(2.5) U.L.
Q_a — Q_d	Register Complementary Outputs (Note b)	10 U.L.	5(2.5) U.L.

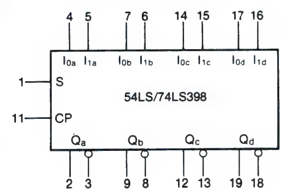
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = 16
GND = 8

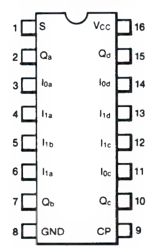
LOGIC SYMBOL



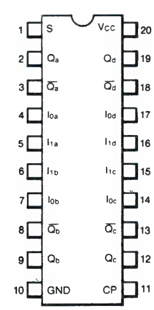
V_{CC} = Pin 20
GND = Pin 10

5

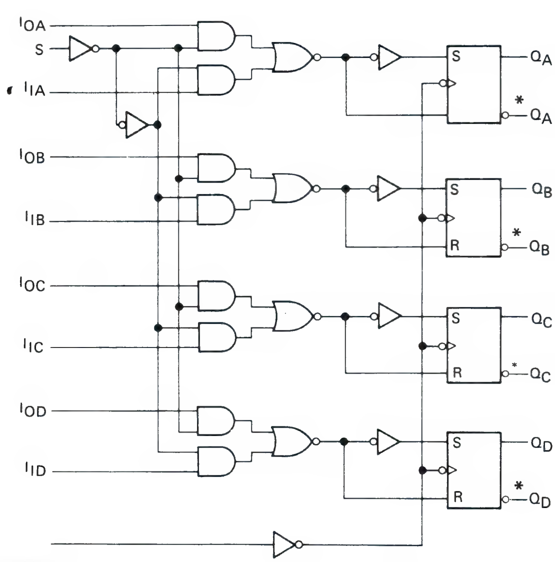
CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS399



CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS398



FUNCTIONAL BLOCK DIAGRAM



* 54LS/74LS398 only

FUNCTIONAL DESCRIPTION — The 54LS/74LS398 and 54LS/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 54LS/74LS398 has both Q and Q Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

* 54LS/74LS398 ONLY

l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURES
	MIN	TYP	MAX	
54LS398 54LS399	4.5 V	5.0 V	5.5 V	-55° C to +125° C
74LS398 74LS399	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			7.3	13	mA	V_{CC} = MAX	

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output Q			27 32	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to $\overline{Q}$ (LS398 only)			27 32	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$t_{w(H)}$	Clock Pulse Width (HIGH)	20			ns	Fig. 1	$V_{CC} = 5.0$ V
$t_{w(L)}$	Clock Pulse Width (LOW)	20			ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	0			ns		
$t_{s(S)}$	Set-up Time, Select to Clock	25			ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

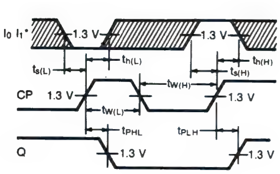


Fig. 1

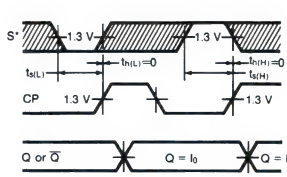


Fig. 2

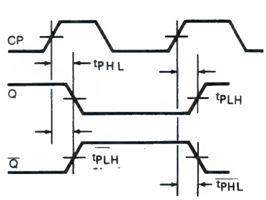


Fig. 3

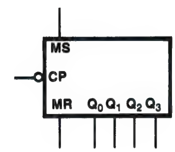
*The shaded areas indicate when the input is permitted to change for predictable output performance.

F54LS/74LS490
DUAL DECADE COUNTER

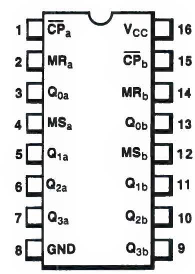
DESCRIPTION – The 54LS/74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the 54LS/74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8, 4, 2, 1 BCD code.

- **DUAL VERSION OF 54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY – TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL
(EACH HALF)



CONNECTION DIAGRAM
DIP (TOP VIEW)



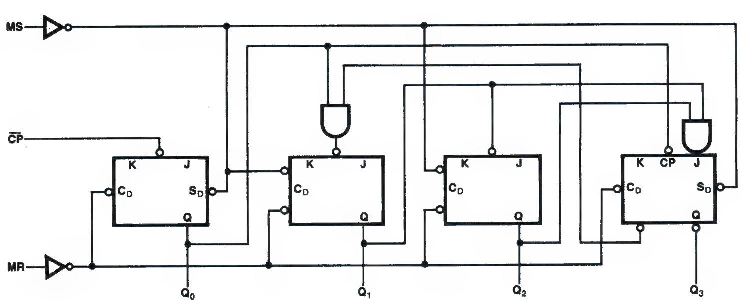
PIN NAMES		**LOADING** (Note a) HIGH	LOW
MS	Master Set (Set to 9) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Input (Active LOW Going Edge)	1.5 U.L.	1.5 U.L.
Q_0-Q_3	Counter Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (XM) and 5 U.L. for COMMERCIAL (XC) Temperature Ranges.

TRUTH TABLE

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LOGIC DIAGRAM (ONE HALF SHOWN)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS490XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS490XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.5			V	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		XC	2.7					
V_{OL}	Output LOW Voltage	XC, XM		0.25	0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5		I_{OL} = 8 mA	
I_{IH}	Input HIGH Current MR, MS $\overline{CP}$				20 60	μA μA	V_{CC} = MAX V_{IN} = 2.7 V	
	$\overline{CP}$ MR, MS				−300 100	μA μA	V_{IN} = 5.5 V $\overline{CP}$ only V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current $\overline{CP}$ MR, MS				−2.4 −0.4	mA mA	V_{CC} = MAX V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			19	26	mA	V_{CC} = MAX	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_w	$\overline{CP}$, MR or MS Pulse Width	20	14		ns	Figs. 1, 2, 3	V_{CC} = 5.0 V
t_{rec}	MR or MS to $\overline{CP}$	15	12		ns	Figs. 2, 3	

DEFINITION OF TERMS:

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the MS or MR pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH Data to the Q outputs.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Input Count Frequency	40	65		MHz	Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ $R_L = 2\ k\Omega$
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0		5.0 6.0	15 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_1 or Q_3		17 19	30 30	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2		25 26	45 45	ns	Fig. 2	
t_{PHL}	Propagation Delay, MR to Output		27	39	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, MS to Output		13 20	35 35	ns	Fig. 2	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at $V_{CC} = 5.0\ V$, $T_A = 25°C$, and maximum loading.
5. Not more than one output should be shorted at a time.

AC WAVEFORMS

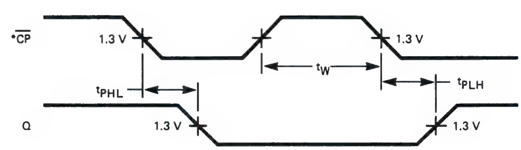


Fig. 1

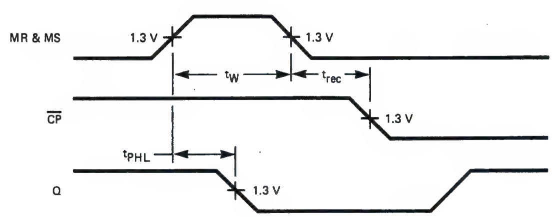


Fig. 2

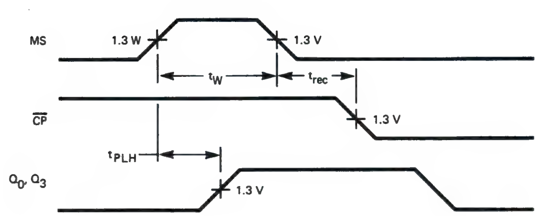


Fig. 3

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.

F54LS/74LS502

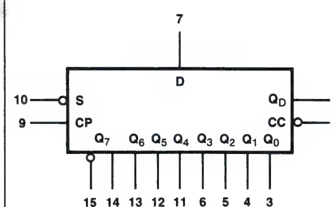
8-BIT SUCCESSIVE APPROXIMATION REGISTER

DESCRIPTION – The 54LS/74LS502 is an 8-Bit Register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete (CC) signal coincident with storage of the eighth bit. An active LOW Start (S) input performs synchronous initialization which forces Q_7 LOW and all other outputs HIGH. Subsequent clocks shift this Q_7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q_7, the second bit in Q_6, the third in Q_5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

Designed primarily for use in the successive approximation technique for analog to digital conversion, the 54LS/74LS502 can also be used as a serial to parallel converter, ring counter and as the storage and control element in recursive digital routines.

- **LOW POWER SCHOTTKY VERSION OF 2502**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION**
- **A TO D CONVERTERS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

LOGIC SYMBOL



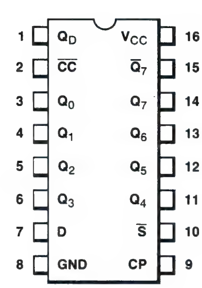
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CC}$	Conversion complete (active LOW) output (note b)	10 U.L.	5(2.5) U.L
CP	Clock Pulse (active HIGH going edge) input	0.5 U.L.	0.25 U.L.
D	Serial Data Input	0.5 U.L.	0.25 U.L.
Q_0–Q_7	Parallel Register Outputs	10 U.L.	5(2.5) U.L.
$\overline{Q_7}$	Complement of Q_7 output	10 U.L.	5(2.5) U.L.
Q_D	Synchronized serial data output	10 U.L.	5(2.5) U.L.
$\overline{S}$	Start (active LOW) input	0.5 U.L.	0.25 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.)=40μA HIGH/1.6mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



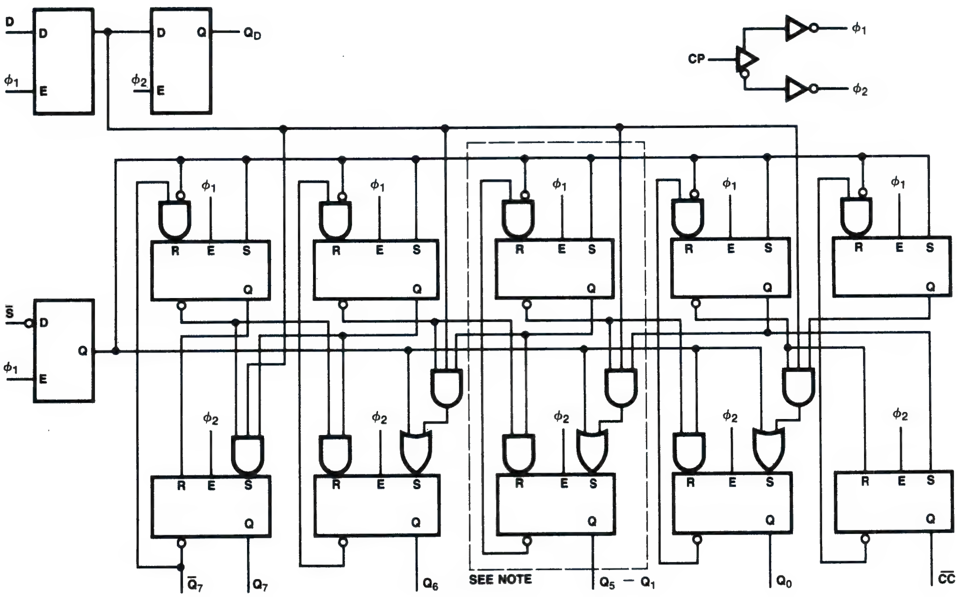
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

FUNCTIONAL DESCRIPTION – The register stages are composed of transparent RS latches arranged in Master/Slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals ϕ_1 and ϕ_2 derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with S remaining LOW, then forces the slave latches to the condition wherein Q_7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q_7, while Q_6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure 1 shows a simplified hook-up of a 54LS/74LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. Figure 2 is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t_1, Q_7 is LOW and Q_6-Q_0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the 54LS/74LS502) will be LOW, and at times t_2 the D/A output will rise to three-fourths of full scale because Q_7 will remain LOW and contribute 50% while Q_6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q_7 will go HIGH at t_2. Q_6 will still be forced LOW at t_2, and the D/A output will decrease to 25% of full scale.

Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t_9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the fullscale output D/A converter.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS/74LS502XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
54LS/74LS502XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TRUTH TABLE

Time	Inputs		Outputs									
t_n	D	$\overline{S}$	Q_D	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	X	L	H	H	H	H	H	H	H	H
2	D_6	H	D_7	D_7	L	H	H	H	H	H	H	H
3	D_6	H	D_6		D_6	L	H	H	H	H	H	H
4	D_4	H	D_5			D_5	L	H	H	H	H	H
5	D_3	H	D_4				D_4	L	H	H	H	H
6	D_2	H	D_3					D_3	L	H	H	H
7	D_1	H	D_2						D_2	L	H	H
8	D_0	H	D_1							D_1	L	H
9	X	H	D_0								D_0	L
10	X	H	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = immaterial

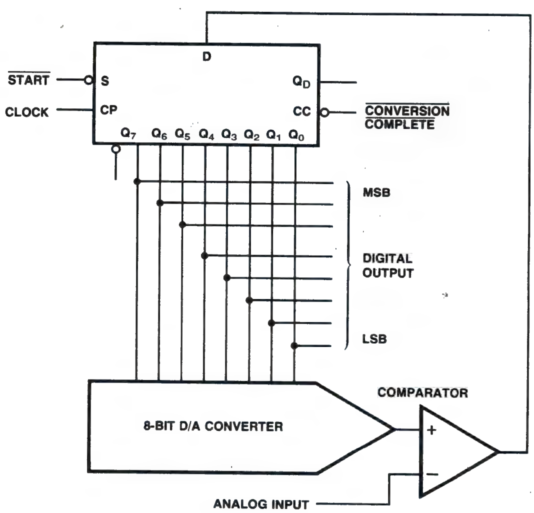


Fig. 1

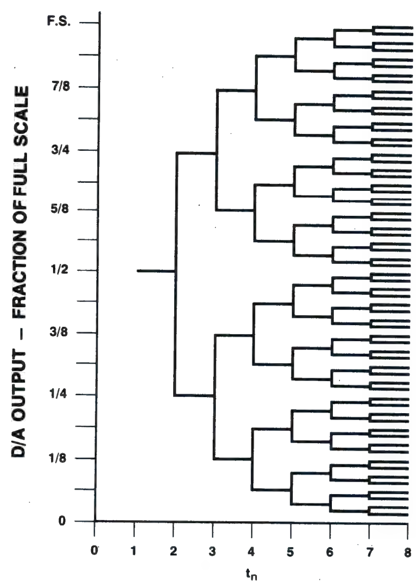


Fig. 2

F54LS/74LS540 • F54LS/74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS540 and the 54LS/74LS541 are similar in function to the 54LS/74LS240 and 54LS/74LS241, respectively, except that Inputs and Outputs are on opposite sides of the package (see Logic Diagram). This pinout arrangement makes these devices especially useful as output ports for the Microprocessors, allowing ease of layout and greater PC board density.

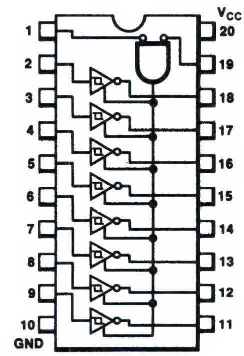
- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGIN**
- **PNP INPUTS REDUCE LOADING**
- **3-STATE OUTPUTS DRIVE BUS LINES**
- **INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIER INTERFACE TO MICROPROCESSORS**
- **INPUT CLAMPDIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

TRUTH TABLE

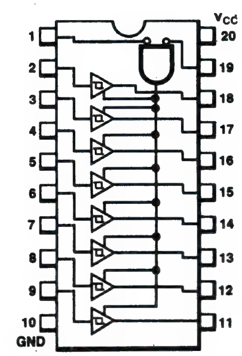
INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM AND CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM AND CONNECTION DIAGRAM
DIP (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS540XM 54LS541XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS540XC 74LS541XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1			I_{OH} = −15 mA	
V_{OL}	Output LOW Voltage	XM, XC		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX. V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX. V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX. V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX. V_{OUT} = 0 V	
I_{CC}	Power Supply Current	54LS/74LS540		29	50	mA	V_{CC} = MAX. V_{IN} = 0 V, V_E = 4.5 V	
		54LS/74LS541		32	54			

NOTES:
1. For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS540			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay Data to Output 54LS/74LS541			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

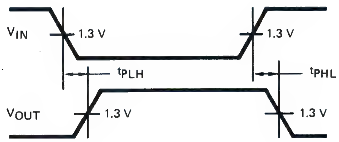


Fig. 1

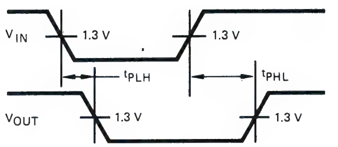


Fig. 2

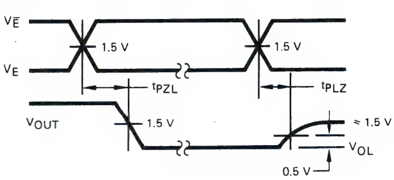


Fig. 3

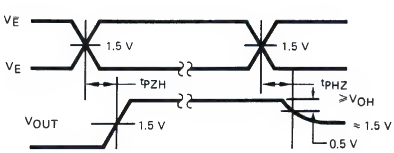
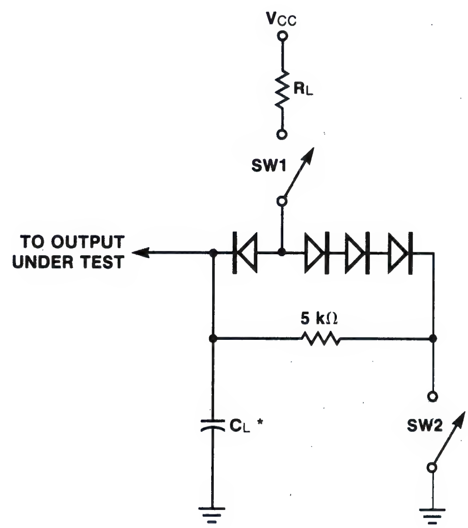


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

F54LS/74LS568 • F54LS/74LS569

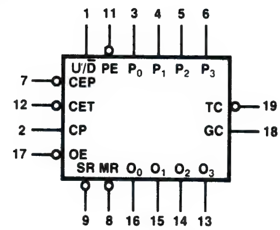
UP/DOWN DECADE COUNTER • UP/DOWN BINARY COUNTER WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS568 and the 54LS/74LS569 are 4-Stage Programmable Up/Down BCD and Binary Counters respectively. Each counter features both a Synchronous Reset ($\overline{SR}$) and an Asynchronous Master Reset ($\overline{MR}$), a single Up/Down ($U/\overline{D}$) control and 3-state outputs for bus organized systems. Both counters are fully edge-triggered, with all functions except Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) synchronized to the LOW-to-HIGH transition of the Clock (CP) input.

Function and operation of these counters is similar to the 54LS/74LS168 and the 54LS/74LS169.

- **FULLY SYNCHRONOUS OPERATION**
- **FULL CARRY LOOKAHEAD FOR EASY CASCADING**
- **SINGLE UP/DOWN CONTROL INPUT**
- **FULL PRESET CAPABILITY**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES TO LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

PIN NAMES / **LOADING** (Note a)

PIN NAMES		HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CET}$	Count Enable Trickle (active LOW) Input	1.0 U.L.	0.5 U.L.
CP	Clock Pulse (active positive going edge) Input	0.5 U.L.	0.25 U.L.
GC	Gated Clock Output (note b)	10.0 U.L.	0.5 (2.5) U.L.
$\overline{MR}$	Asynchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	3-State Output Enable (active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Input	0.5 U.L.	0.25 U.L.
$\overline{PE}$	Parallel Enable (active LOW) Input	0.5 U.L.	0.25 U.L.
O_n	Flip-Flop outputs (note b)	65 (25) U.L.	15 (7.5) U.L.
$\overline{TC}$	Terminal Count (active LOW) Output (note b)	10 U.L.	5 (2.5) U.L.
$\overline{SR}$	Synchronous Reset (active LOW) Input	1.0 U.L.	0.5 U.L.
$U/\overline{D}$	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FUNCTION TABLE

INPUTS							RESPONSE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous RESET; Q_n = LOW
H	L	X	X	X	X	↑	Synchronous RESET; Q_n = LOW
H	H	L	X	X	X	↑	Parallel Load; $P_n \rightarrow Q_n$
H	H	H	H	X	X	X	Hold
H	H	H	X	H	X	X	Hold
H	H	H	L	L	H	↑	Count Up
H	H	H	L	L	L	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GC TRUTH TABLE

INPUTS				GC OUTPUT
$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	
L	L	L	⊔	⊔
H	X	X	X	H
X	H	X	X	H
L	L	H	X	H

*TC is generated internally.

5

F54LS/74LS573

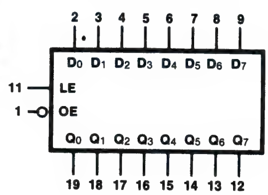
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

GENERAL DESCRIPTION — The 54LS/74LS573 is a High-Speed Octal Latch with Buffered Common Latch Enable (LE) and Buffered Common Output Enable (OE) inputs.

This device is functionally identical to the 54LS/74LS373, but has different pinouts. For truth tables, discussion of operations and AC and DC specifications, please refer to the 54LS/74LS373 Data Sheet.

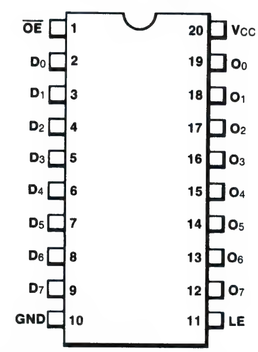
- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 54LS/74LS373**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

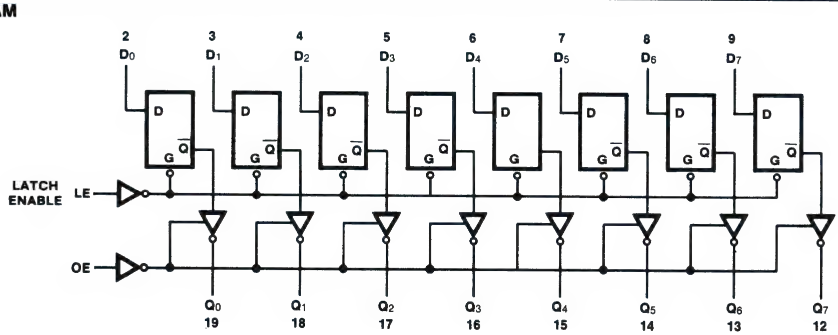


PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0 - D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0 - O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH 1.6 mA LOW
b) The Output LOW drive factor is 7.5 U.L. for Military (XM) and 15 U.L. for Commercial (XC) Temperature Ranges. The Output HIGH drive factor is 25 U.L. Military (XM) and 65 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
0 = Pin numbers

F54LS/74LS574

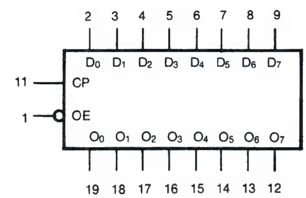
OCTAL D FLIP-FLOP WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS574 is a high-speed low-power Octal Flip-Flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 54LS/74LS374 except for the pinouts. For complete discussions of operations, truth tables, AC and DC electrical specifications, refer to the 54LS/74LS374 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 54LS/74LS374**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



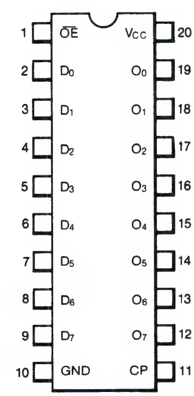
V_{CC} = Pin 20
GND = Pin 10

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 — D_7$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$O_0 — O_7$	Outputs (Note b)	65(25) U.L.	15(7.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The output LOW drive factor is 7.5 U.L. for military (XM) and 15 U.L. for Commercial (XC) temperature ranges. The output HIGH drive factor is 25 U.L. for Military (XM) and 65 U.L. for Commercial (XC) temperature ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

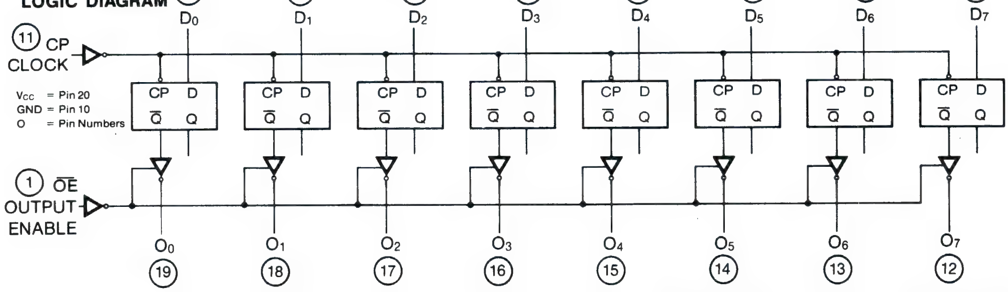
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
54LS574XM	4.5 V	5.0 V	5.5 V	-55° C to +125° C
54LS574XC	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

LOGIC DIAGRAM



F54LS/74LS670

4 × 4 REGISTER FILE WITH 3-STATE OUTPUTS

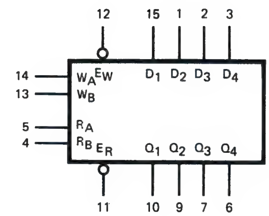
DESCRIPTION — The 54LS/74LS670 contains 16 high-speed, low-power transparent D-type latches arranged as four words of four bits each, to function as a 4 × 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The 54LS/74LS170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

LOGIC SYMBOL



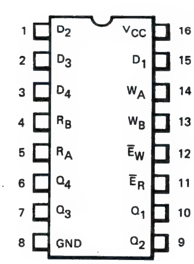
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\bar{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\bar{E}_R$	Read Enable (Active LOW) Input	1.5 U.L.	0.75 U.L.
Q_1–Q_4	Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

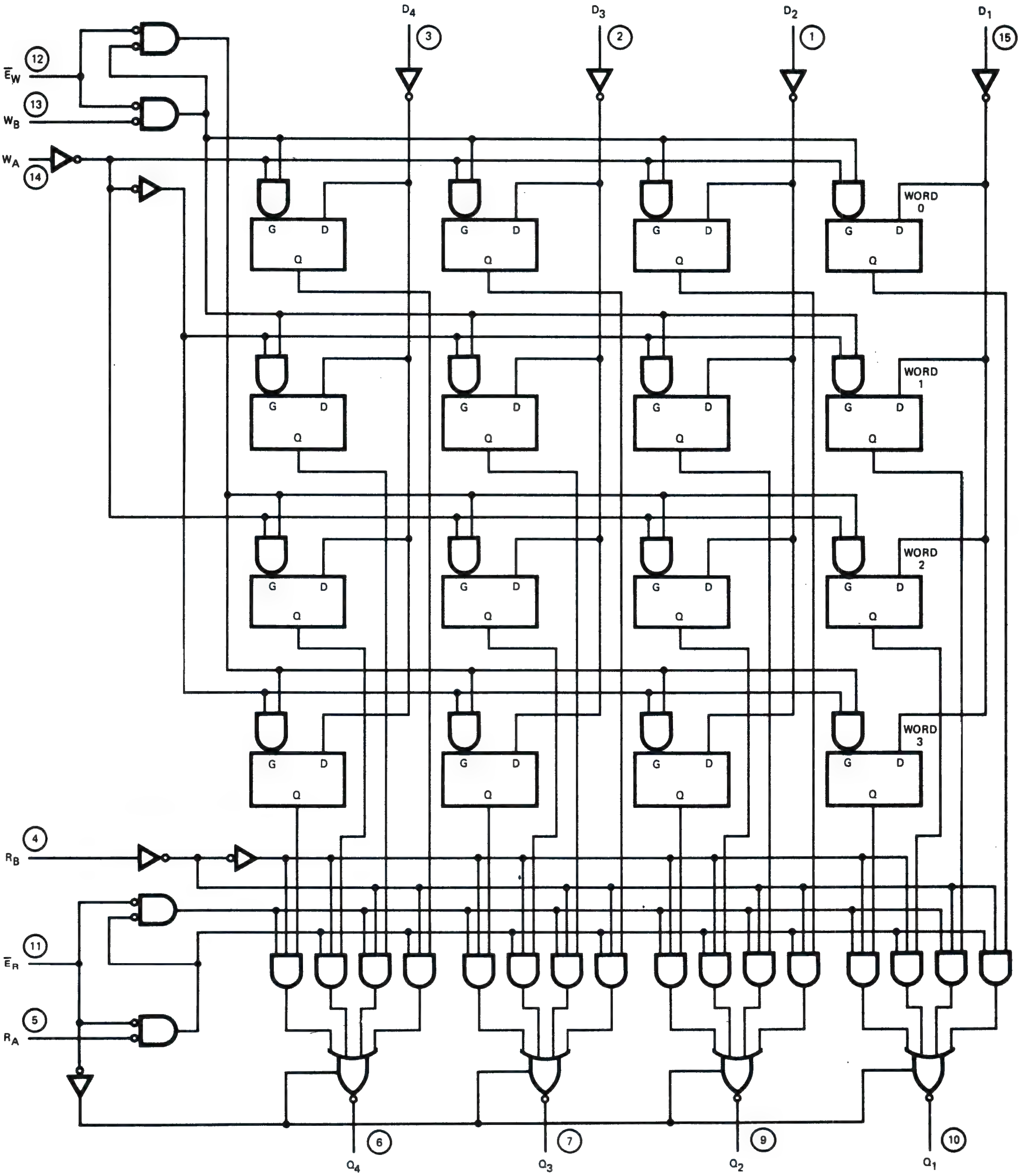
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
54LS670XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
74LS670XC	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, V_{IH} = 2 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_{IH} = 2 V	
I_{IH}	Input HIGH Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$				20 40 60	μA	V_{CC} = MAX, V_{IN} 2.7 V	
	Any D, R or W $\overline{E}_W$ $\overline{E}_R$				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$				−0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 5)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			30	50	mA	V_{CC} = MAX (Note 6)	

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.
6. Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay R_A or R_B to Q Outputs			40 45	ns	Fig. 2	$V_{CC} = 5$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\bar{E}_W$ to Q Outputs			45 50	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 40	ns	Fig. 1	
t_{PZH}	Enable Time, Negative Going $\bar{E}_R$ to Q Outputs Going HIGH			35	ns	Fig. 4,5	$V_{CC} = 5$ V $C_L = 5.0$ pF $R_L = 2$ kΩ See Page 5-98 for 3-state Waveforms (Figs. 3,4,5)
t_{PZL}	Enable Time, Negative Going $\bar{E}_R$ to Q Outputs Going LOW			40	ns	Fig. 3,5	
t_{PHZ}	Disable Time, Positive Going $\bar{E}_R$ to Q Outputs Off from HIGH			50	ns	Fig. 4,5	
t_{PLZ}	Disable Time, Positive Going $\bar{E}_R$ to Q Outputs Off from LOW			35	ns	Fig. 3,5	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\bar{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 6 (Note 10)
t_sD (Note 7)	Set-Up Time, Data Inputs with Respect to Positive-Going $\bar{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\bar{E}_W$	15			ns	
t_sW (Note 9)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\bar{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\bar{E}_W$	5			ns	

NOTES:
7. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW-to-HIGH in order for the latch to recognize and store the new data.
8. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
9. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
10. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

AC WAVEFORMS

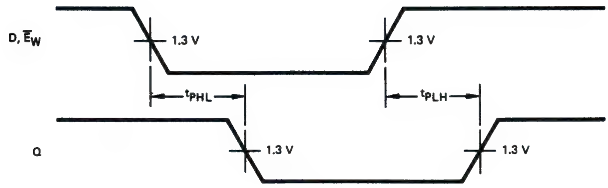


Fig. 1

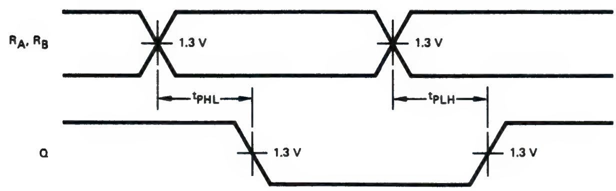


Fig. 2

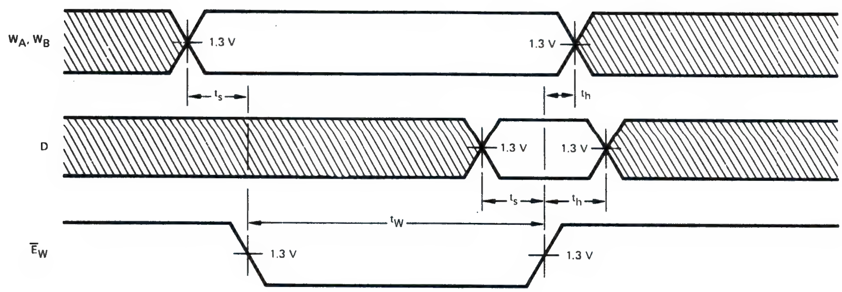


Fig. 6

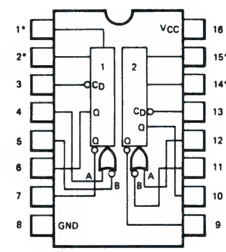
F96L02

LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The TTL/Monostable 96L02 is a low-power Dual Retriggerable, Resettable Monostable Multivibrator which provides andoutput pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

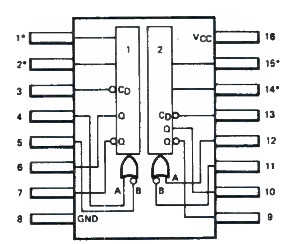
- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100 % DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE-TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

CONNECTION DIAGRAM
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)



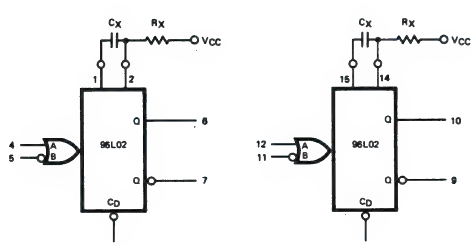
*Pins for external timing.

PIN NAMES

		LOADING HIGH	LOADING LOW
B	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
C_D	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
Q	Output (Active LOW)	9.0	3.0

1 Unit Load (U.L.) = 40µA HIGH/1.6 mA LOW

LOGIC DIAGRAM

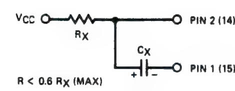


FUNCTIONAL DESCRIPTION – The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active level LOW input or the Q output to the active level HIGH input.

OPERATION RULES

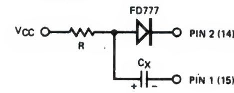
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for –55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows: $t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right]$ (for $C_X > 10^3$ pF) Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 1
5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 μA, and the inverse capacitor leakage at 1.0 V is less than 1.6 μA over the operational temperature range and Rule 3 above is satisfied.



   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\, RC_X$$



   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

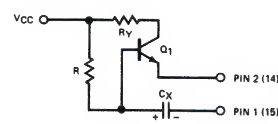
   $R < R_X\,(0.7)\,(h_{FE}\,Q_1)$ or < 2.5 MΩ whichever is the lesser

   $R_X\,(\min) < R_Y < R_X\,(\max)$

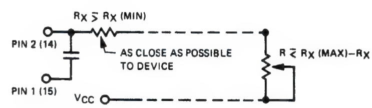
   Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\, RC_X$$

   This configuration is not recommended with retriggerable operation.

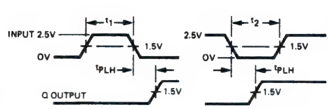


6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

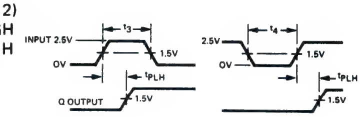


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

   Input to Pin 5 (11)
   Pin 4 (12) = LOW
   Pin 3 (13) = HIGH
   t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
   t_2, t_4 = Min. Negative Input Pulse Width > 60 ns

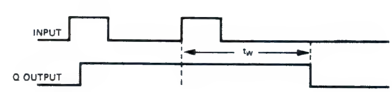


   Input to Pin 4 (12)
   Pin 5 (11) = HIGH
   Pin 3 (13) = HIGH



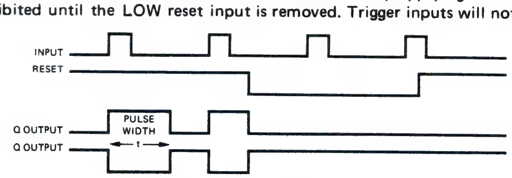
9. The retriggerable pulse width is calculated as shown below:

$$t_w = t + t_{PLH} = 0.33\ R_X\ C_X\ \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



   The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation – An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
96L02XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; F for Flatpak, D for Ceramic Dip.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 4)	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	V	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		V	V_{CC} = MIN., I_{OH} = −0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	V	V_{CC} = MIN., I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−2.0		−13	mA	V_{CC} = MAX., V_{OUT} = 1.0 V
I_{CC}	Power Supply Current		10	16	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
96L02XM						
t_{PLH}	Negative Trigger Input to True Output		55	75	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Negative Trigger Input to Complement Output		45	62	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	µs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	$R_X = 39$ kΩ, $C_X = 1000$ pF
96L02XC						
t_{PLH}	Negative Trigger Input to True Output		55	80	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Negative Trigger Input to Complement Output		45	65	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	µs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	$R_X = 39$ kΩ, $C_X = 1000$ pF

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X ($C_X \leq 1000$ pF)
(FOR $C_X > 1000$ pF SEE OPERATION RULES 4 AND 5.)

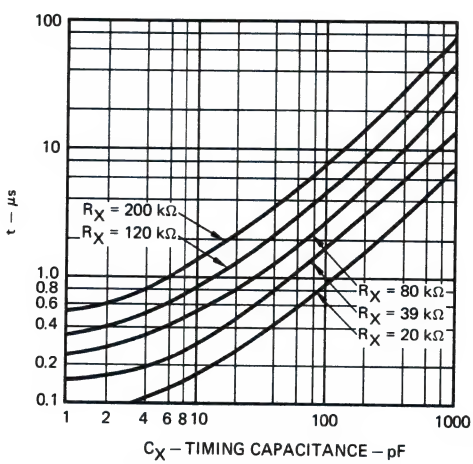
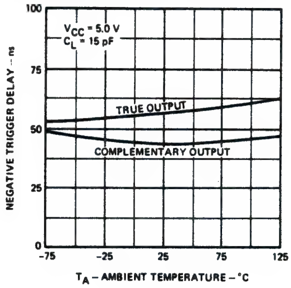


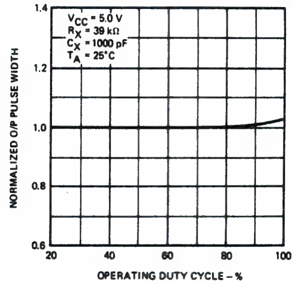
Fig. 1

TYPICAL PULSE CHARACTERISTICS

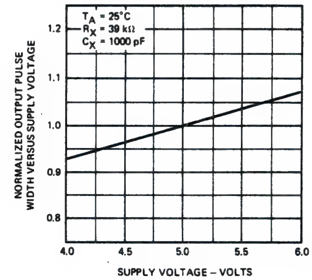
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



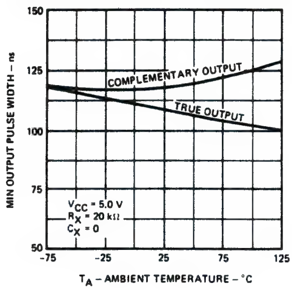
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



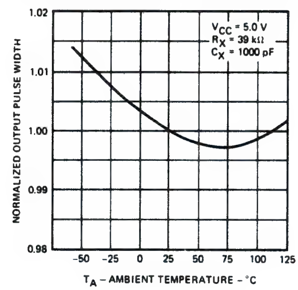
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MIN. OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



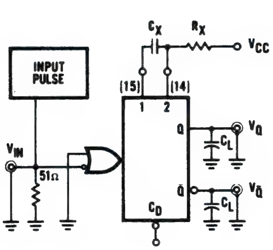
5

TRIGGERING TRUTH TABLE

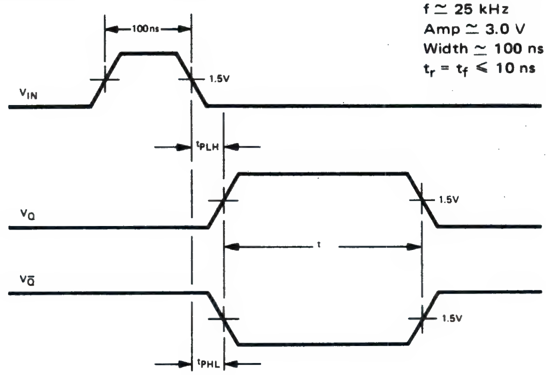
PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ⩾ V_{IH}
L = LOW Voltage Level ⩽ V_{IL}
X = Immaterial
H→L = HIGH-to-LOW Voltage Level transition
L→H = LOW-to-HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8



INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leqslant 10$ ns

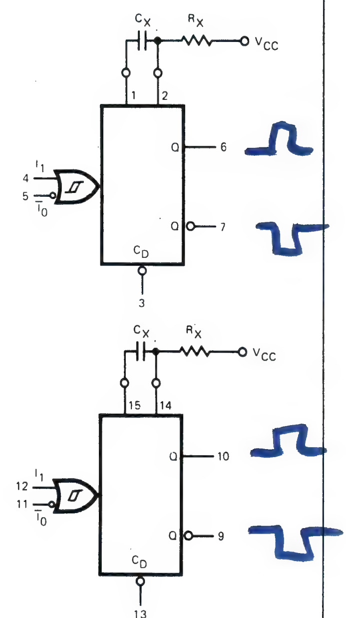
F96S02

LOW POWER SCHOTTKY DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The 96S02 is a Dual Retriggerable and Resettable Monostable which uses Schottky technology to provide wide delay range, stability, prediction accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. The 96S02 may utilize timing resistors to 2 MΩ thus reducing required capacitor values. Hysteresis is provided on the positive-going inputs for increased noise immunity. The 96S02 is fully compatible with all TTL families.

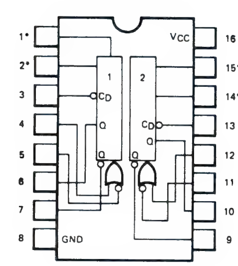
- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.5 kΩ TO 2 MΩ**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 1300:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 12 ns**
- **OUTPUT PULSE WIDTH STABILITY OF 0.2% OVER 0°C to 75°C TEMPERATURE RANGE**
- **OUTPUT PULSE WIDTH STABILITY OF ±0.3% OVER 4.75 V TO 5.25 V POWER SUPPLY RANGE**
- **PULSE WIDTH VARIATION OF ±5% FROM UNIT TO UNIT**
- **0.3 V HYSTERSIS ON BOTH TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **27 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RESETTABLE IN 9 ns**
- **SAME PINOUT AS 9602, 96L02, 96LS02**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



*Pins for external timing.

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{I}_0$	Trigger (Active LOW) Input	0.5 U.L.	0.625 U.L.
I_1	Schmitt Trigger (Active HIGH) Input	0.5 U.L.	0.625 U.L.
$\overline{C}_D$	Clear (Active LOW) Input	0.5 U.L.	0.625 U.L.
Q	Pulse (Active HIGH) Output (Note b)	25 U.L.	12.5 U.L.
$\overline{Q}$	Pulse (Active LOW) Output (Note b)	25 U.L.	12.5 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

FUNCTIONAL DESCRIPTION — The 96S02 Schottky Dual Retriggerable Resettable Monostable Multivibrator has two dc coupled trigger inputs per function, one active LOW ($\overline{I_0}$) and one active HIGH (I_1). The I_1 input utilizes an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either leading or trailing edge-triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the 96S02 and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I_0}$ or the Q output to I_1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from init to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families. High impedance inputs minimize loading and provide compatibility with low power families such as 54LS/74LS.

OPERATION RULES

TIMING

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.5 kΩ to 2 MΩ.

2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.

3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (−) terminal to pin 2 (14) and R_X. Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle; however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to 2 (14) depending on values of R_X and V_{CC}. For values of $R_X \geqslant 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVDC or higher should be used when $R_X \geqslant 10$ kΩ.

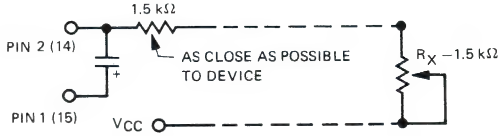
4. The output pulse width t_W for $R_X \geqslant 10$ kΩ and $C_X \geqslant 100$ pF is determined as follows:

$$\boxed{t_W = 0.5\ R_X C_X}$$

Where R_X is in kΩ, C_X is in pF, t is in ns OR R_X is in kΩ, C_X is in µF, t is in ms

5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

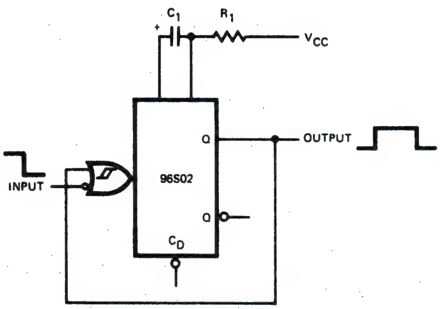


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

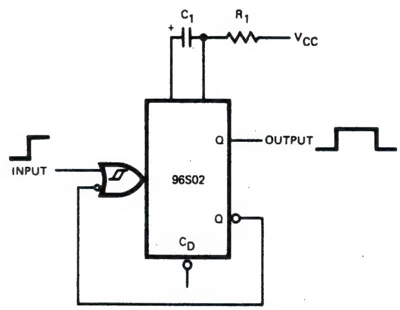
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 µF bypass capacitor between V_{CC} and ground located near the 96S02 is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I_0}$ is 8 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



NEGATIVE EDGE-TRIGGER



POSITIVE EDGE-TRIGGER

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on C_D will *not* trigger the 96S02.

TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	96S02XC MIN	TYP	MAX	UNITS
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Operating Free-Air Temperature Range	0	25	75	C
Input Loading for Each Input			0.625	U.L.
Fan-out	12.5			U.L.

X = package type; D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage Except Pins 4 & 12	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage Except Pins 4 & 12			0.8	V	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		−0.65	−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{T+}	Positive-Going Threshold Voltage, Pins 4 & 12		1.7	2.0	V	V_{CC} = 5.0 V, T_A = 25°C
V_{T-}	Negative-Going Threshold Voltage, Pins 4 & 12	0.8	1.4		V	V_{CC} = 5.0 V, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.7	3.2		V	V_{CC} = MIN, I_{OH} = −1.0 mA, V_{IN} = 0.8 V
V_{OL}	Output LOW Voltage		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}
I_{IH}	Input HIGH Current		0.2	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
				0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.6	−1.0	mA	V_{CC} = MAX, V_{IN} = 0.5 V
V_{CX}	Capacitor Voltage, Pin 1 (15) Referenced to Pin 2 (14)	−0.85		3.0	V	R_X = 1.5 kΩ; V_{CC} = 4.75 V to 5.25 V
		−0.5		3.0	V	$R_X \geq$ 10 kΩ; V_{CC} = 4.75 V to 5.25 V
		−0.4		3.0	V	$R_X \geq$ 1 MΩ; V_{CC} = 4.75 V to 5.25 V
I_{OS}	Output Short Circuit Current (Note 3)	−40	−65	−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Quiescent Power Supply Drain		48	70	mA	Inputs Open

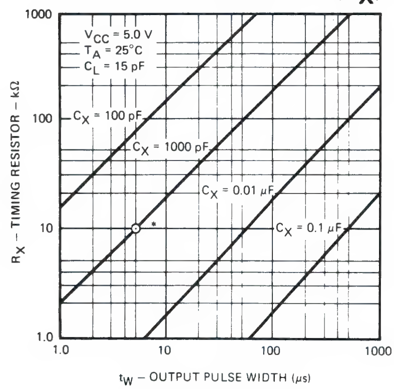
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
t_{PLH}	Negative Trigger Input to True Output		10	15	ns	
t_{PHL}	Negative Trigger Input to Complement Output		12	19	ns	
t_{PLH}	Positive Trigger Input to True Output		12	19	ns	
t_{PHL}	Positive Trigger Input to Complement Output		15	20	ns	
t_{PHL}	Clear Input to True Output		6.5	10	ns	
t_{PLH}	Clear Input to Complement Output		9.0	14	ns	
$t_{W(MIN)}$	Min. Negative Trigger Pulse Width on $\overline{I_0}$		3.0	8.0	ns	
$t_{W(MIN)}$	Min. Positive Trigger Pulse Width on I_1		7.0	12	ns	
$t_{W(MIN)}$	Min. Clear Pulse Width		3.0	7.0	ns	
$t_{W(MIN)}$	Min. True Output Pulse Width	22	27	35	ns	R_X = 1.5 kΩ, C_X = stray capacity only
$t_{W(MIN)}$	Min. True Output Pulse Width	30	38	45	ns	R_X = 1.5 kΩ, C_X = 10 pF including stray and jig capacitance
t_W	True Output Pulse Width	4.9	5.2	5.5	μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	1.5		2000	kΩ	T_A = 0°C to 75°C, V_{CC} = 4.75 V to 5.25 V
Δt	Max. Change in True Output Pulse Width over Temperature Range		0.38	1.0	%	T_A = 0°C to 75°C, V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
Δt	Max. Change in True Output Pulse Width over V_{CC} Range		0.38	1.0	%	T_A = 25°C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF

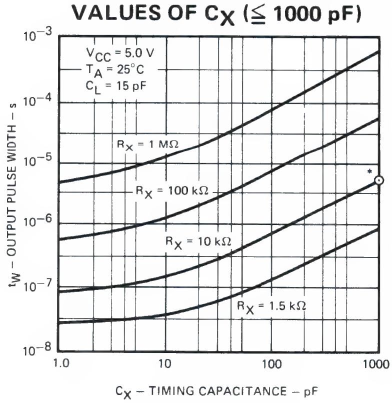
TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR (R_X) AND TIMING CAPACITOR (C_X)



*Guaranteed Limits are 4.9 μs to 5.5 μs.

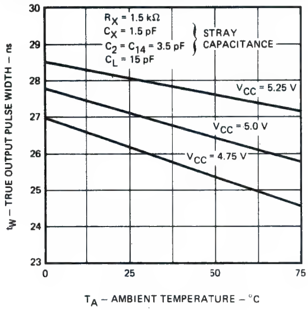
OUTPUT PULSE WIDTH VERSUS TIMING CAPACITANCE FOR LOW VALUES OF C_X (≦ 1000 pF)



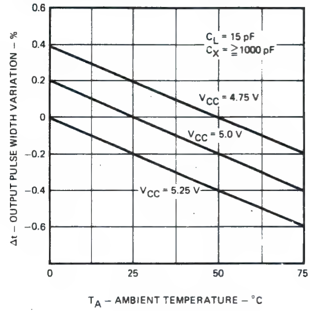
*Guaranteed Limits are 4.9 μs to 5.5 μs.

TYPICAL CHARACTERISTICS (Cont'd)

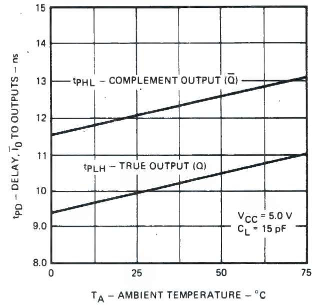
MINIMUM OUTPUT PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE (NO EXTERNAL TIMING CAPACITOR)



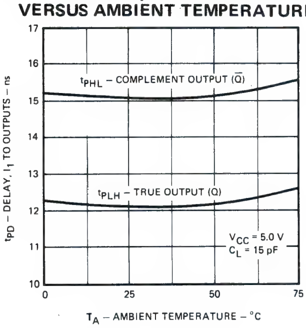
NORMALIZED OUTPUT PULSE WIDTH VARIATION VERSUS AMBIENT TEMPERATURE



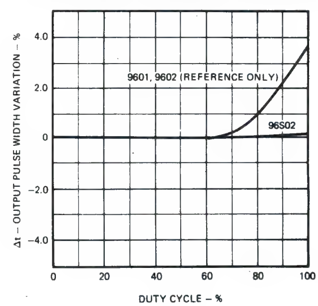
DELAY FROM NEGATIVE TRIGGER INPUT $\overline{I}_0$ TO OUTPUTS VERSUS AMBIENT TEMPERATURE



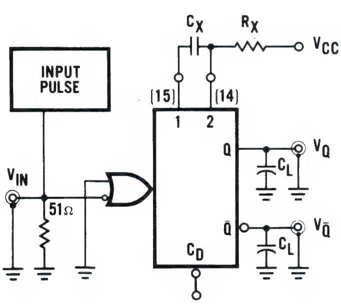
DELAY FROM POSITIVE TRIGGER INPUT I_1 TO OUTPUTS VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VARIATION VERSUS DUTY CYCLE

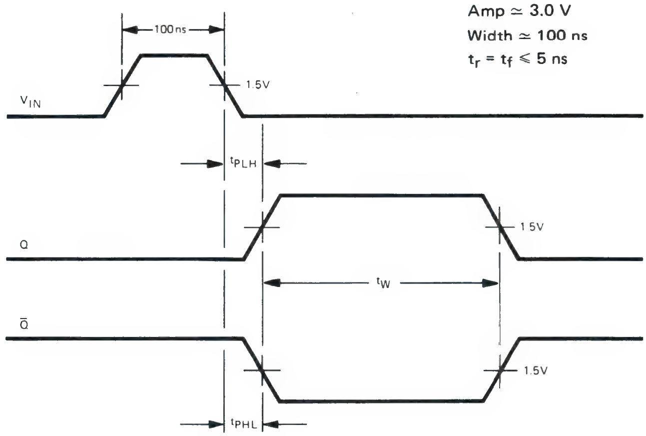


AC CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 5$ ns



5

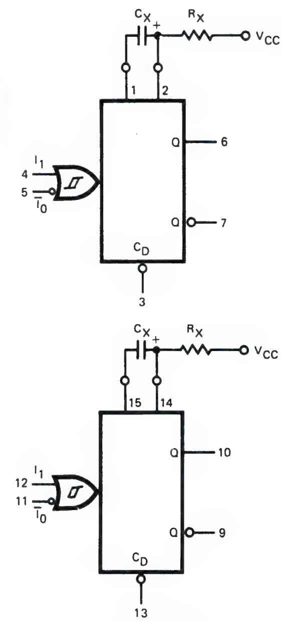
F96LS02

LOW POWER SCHOTTKY DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The 96LS02 is a Dual Retriggerable and Resettable Monostable which uses Low Power Schottky technology to provide wide delay range, stability, prediction accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. The 96LS02 may utilize timing resistors to 1 MΩ thus reducing required capacitor values. Hysteresis is provided on the inputs for increased noise immunity. The 96LS02 is fully compatible with all TTL families.

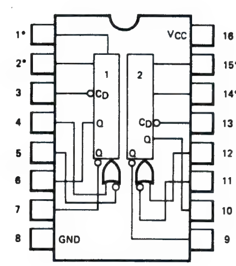
- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1 kΩ to 1 MΩ**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 1300:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns**
- **OUTPUT PULSE WIDTH STABILITY OF ±0.5% OVER 0°C to 70°C TEMPERATURE RANGE**
- **OUTPUT PULSE WIDTH STABILITY OF ±0.7% OVER 4.75 V to 5.25 V POWER SUPPLY RANGE**
- **PULSE WIDTH VARIATION OF ±5% FROM UNIT TO UNIT**
- **0.3 V HYSTERESIS ON BOTH TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RESETTABLE IN 20 ns**
- **SAME PINOUT AS 9602, 96L02, 96S02**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



*Pins for external timing.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{I}_0$	Trigger (Active LOW) Input	0.5 U.L.	0.625 U.L.
I_1	Schmitt Trigger (Active HIGH) Input	0.5 U.L.	0.625 U.L.
$\overline{C}_D$	Clear (Active LOW) Input	0.5 U.L.	0.625 U.L.
Q	Pulse (Active HIGH) Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}$	Pulse (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage Except Pins 4 & 12		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage Except Pins 4 & 12	XC			0.8	V	Guaranteed Input LOW Voltage
		XM			0.7		
V_{CD}	Input Clamp Diode Voltage				-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{T+}	Positive-Going Threshold Voltage, Pins 4 & 12				2.0	V	V_{CC} = 5.0 V, T_A = 25° C
V_{T-}	Negative-Going Threshold Voltage, Pins 4 & 12		0.8			V	V_{CC} = 5.0 V, T_A = 25° C
V_{OH}	Output HIGH Voltage	XC	2.7			V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = 0.8 V
		XM	2.5				
V_{OL}	Output LOW Voltage	XC			0.5	V	V_{CC}=MIN, V_{IN}=V_{IH} or V_{IL}; I_{OL}=8 mA
		XM			0.4		I_{OL}=4 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4
I_{OS}	Output Short Circuit Current (Note 3)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Quiescent Power Supply Drain				35	mA	Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25° C, V_{CC} = 5.0 V, C_L = 15 pF (unless other noted)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
t_{PLH}	Negative Trigger Input to True Output			36	55	ns	R_X = 10 kΩ, C_X = 1000 pF, V_{CC} = 5 V, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output			32	50	ns	
t_{PLH}	Positive Trigger Input to True Output			39	60	ns	
t_{PHL}	Positive Trigger Input to Complement Output			35	55	ns	
t_{PHL}	Clear Input to True Output			19	30	ns	
t_{PLH}	Clear Input to Complement Output			22	35	ns	
$t_{W(MIN)}$	Min. Negative Trigger Pulse Width on $\overline{I_0}$			6	10	ns	
$t_{W(MIN)}$	Min. Positive Trigger Pulse Width on I_1			20	30	ns	
$t_{W(MIN)}$	Min. Clear Pulse Width			17	22	ns	
$t_{W(MIN)}$	Min. True Output Pulse Width			38		ns	R_X = 1 kΩ, C_X = stray capacity only
t_W	True Output Pulse Width			7		μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range		1		1000	kΩ	T_A = 0° C to 70° C, V_{CC} = 4.75 V to 5.25 V
Δt	Max. Change in True Output Pulse Width over Temperature Range	XC		0.5	1.0	%	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
		XM		1.5	3.0		
Δt	Max. Change in True Output Pulse Width over V_{CC} Range			0.7	1.0	%	T_A = 25° C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF
				1.5	3.0		T_A = 25° C, V_{CC} = 4.5 to 5.5 V, R_X = 10 kΩ, C_X = 1000 pF

5

FUNCTIONAL DESCRIPTION — The 96LS02 Schottky Dual Retriggerable Resettable Monostable Multivibrator has two dc coupled trigger inputs per function, one active LOW ($\overline{I_0}$) and one active HIGH (I_1). Both inputs utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either leading or trailing edge-triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the 96LS02 and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I_0}$ or the Q output to I_1.

OPERATION RULES

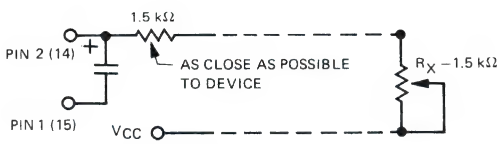
TIMING

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1 kΩ to 1 MΩ.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 2 (14), the (-) terminal to pin 1 (15) and R_X. Pin 2 (14) will remain positive with respect to pin 1 (15) during the timing cycle.
4. The output pulse width t_W for $R_X \geq 10$ kΩ and $C_X \geq 100$ pF is determined as follows:

$$\boxed{t_W = 0.7\,R_X C_X}$$

Where R_X is in kΩ, C_X is in pF, t is in ns OR R_X is in kΩ, C_X is in µF, t is in ms

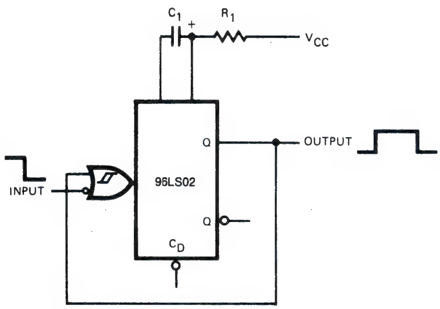
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



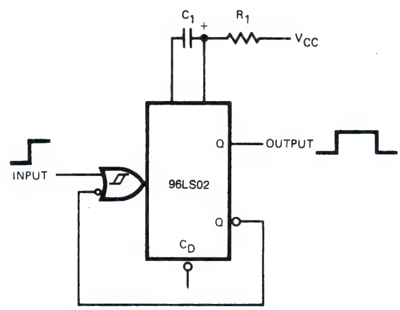
7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 µF bypass capacitor between V_{CC} and ground located near the 96LS02 is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I_0}$ is 8 ns; the minimum positive pulse trigger input I_1 is 12 ns.
2. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



NEGATIVE EDGE TRIGGER



POSITIVE EDGE TRIGGER

3. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on C_D will *not* trigger the 96LS02.

TRIGGERING TRUTH TABLE

PIN NO'S.			OPERATION
5(11)	4(12)	3(13)	
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+50 mA

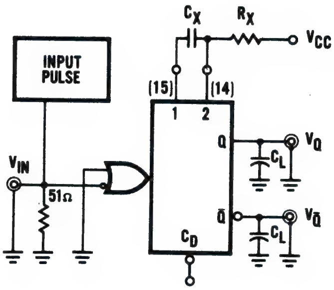
*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	96LS02			UNITS
	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Operating Free-Air Temperature Range	0	25	75	C

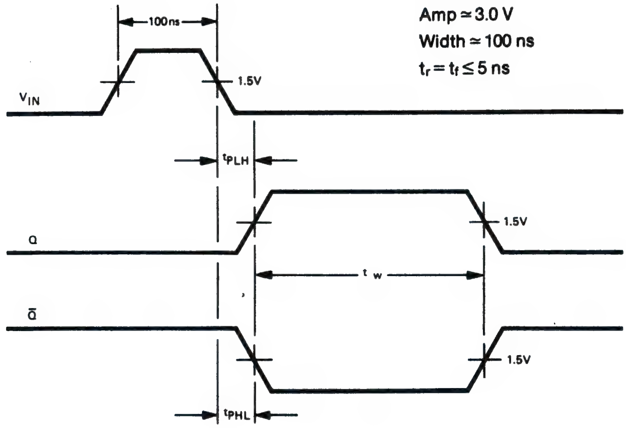
5

AC CIRCUITS AND WAVEFORMS



VCC = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 5$ ns



F96LS32

ADDRESS MULTIPLEXER/REFRESH COUNTER FOR 4K DYNAMIC RAMS

DESCRIPTION — The 96LS32 is an Address Multiplexer and Refresh Counter for multiplexed address dynamic RAMS requiring refresh of up to six input addresses (or 4K bits for 64 × 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6-bit refresh counter which is externally clocked so that either distributed or burst refresh may be used. The high performance of the 96LS32 makes it especially suitable for use with high-speed N-channel RAMS like the F4027.

The 96LS32 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

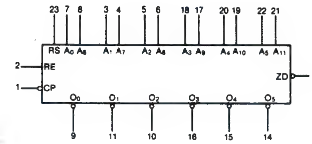
- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITANCE LOADS**
- **USE FOR DISTRIBUTED OR BURST REFRESH**
- **STANDARD 24-PIN DIP**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0-A_5	Row Address Inputs	0.5 U.L.	0.13 U.L.
A_6-A_{11}	Column Address Inputs	0.5 U.L.	0.13 U.L.
CP	Clock Pulse (active negative going edge)input	0.5 U.L.	0.13 U.L.
O_0-O_5	Address Outputs	25 U.L.	3.1 U.L.
RE	Refresh Enable (active HIGH) input	0.5 U.L.	0.13 U.L.
RS	Row Select (active HIGH) input	0.5 U.L.	0.13 U.L.
ZD	Refresh Counter Zero Detect (active LOW) output	25 U.L.	3.1 U.L.

NOTE:
a. 1 TTL unit load (U.L.) = 40 uA HIGH/1.6 mA LOW

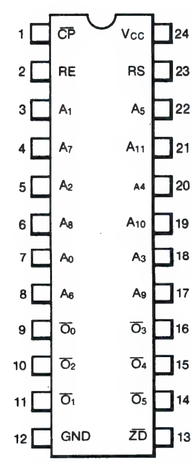
LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

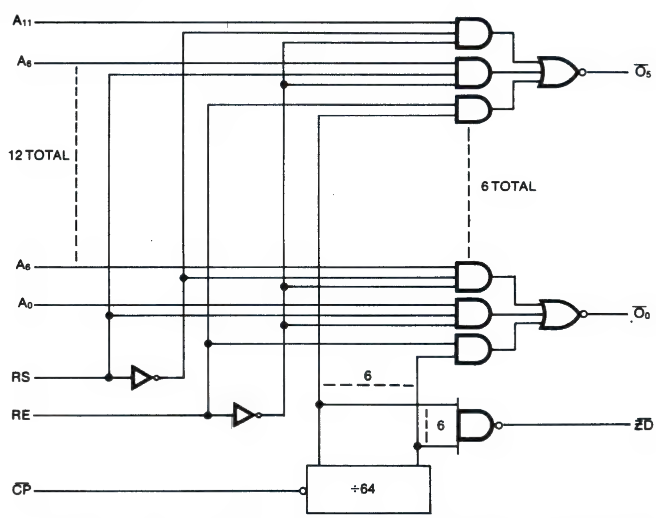
5

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 96LS32 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals Refresh Enable and Row Select both of which are active HIGH TTL inputs. The Function Table shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested the Refresh Enable input is HIGH. This input is ANDed with the six outputs of the internal 6-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs (O_0-O_5) through all 64 row addresses. When the counter sequences to all zeros, the Zero Detect output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after tcz following the LOW going edge of $\overline{CP}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the F4027, Refresh = 2ms and n = 64, therefore one row is refreshed each 31μs. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 96LS32. When Refresh Enable is LOW and Row Select is HIGH, the input Addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW). Input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

When memory devices are driven directly by the 96LS32, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS32. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of A_0-A_5)
L	L	Column Address (complement of A_6-A_{11})

H = HIGH Voltage level L = LOW Voltage level X = Immaterial

AC CHARACTERISTICS: V_{CC} = 5 V @ 25°C

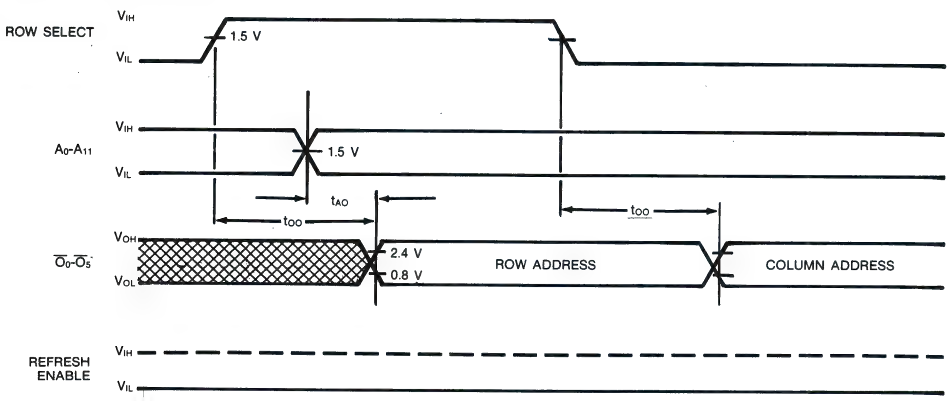
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
t_{AO}	Address Input to output delay		30	ns	CL = 15 pF, RE = LOW
t_{AO1}	Address Input to output delay		37	ns	CL = 250 pF, RE = LOW
T_{OO}	Row Select to output	10	30	ns	CL = 15 pF, RE = LOW
t_{OO1}	Row Select to output	13	37	ns	CL = 250 pF
t_{EO}	Refresh Enable to output	10	30	ns	CL = 15 pF
t_{EO1}	Refresh Enable to output		35	ns	CL = 250 pF
t_{CO}	$\overline{CP}$ to output	10	45	ns	CL = 15 pF, RE = HIGH
t_{CO1}	$\overline{CP}$ to output		50	ns	CL = 250 pF, RE = HIGH
f_C	Count frequency	15		MHz	
t_{CPW}	$\overline{CP}$ pulse width	20		ns	
t_{CZ}	$\overline{CP}$ to $\overline{ZD}$		40	ns	

DC

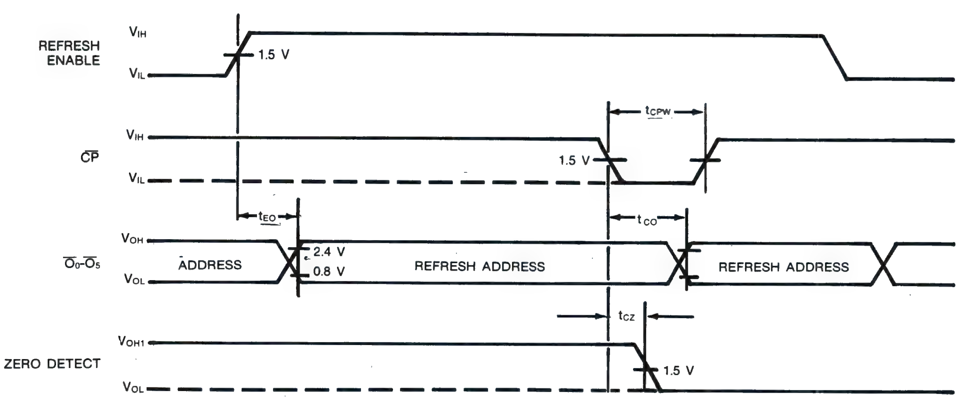
SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
I_{IL}	Input Load Current		-0.2	mA	V_{IN} = 0.4 V, V_{CC} = Max
I_{IH}	Input Leakage Current		20	uA	V_{IN} = 2.7 V, V_{CC} = Max
			100	uA	V_{IN} = 10 V V_{CC} = Max
V_{IL}	Input HIGH Threshold	2		V	
V_{IL}	Input LOW Threshold		0.8	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 5 mA, V_{CC} = Min
V_{OH}	Output HIGH Voltage O_0-O_5	2.8		V	I_{OH} = 1 mA, V_{CC} = Min
V_{OH1}	Output HIGH Voltage $\overline{ZD}$	2.4		V	I_{OH} = 1 mA, V_{CC} = 5.5 V
V_{CD}	Input Clamp Voltage		-1.5	V	V_{CC} = Min, I_{IN} = -18 mA

A.C. TIMING WAVEFORMS

NORMAL CYCLE



REFRESH CYCLE

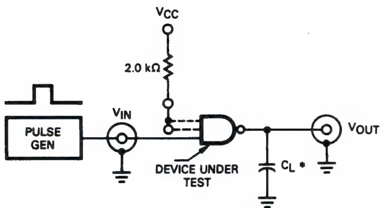


= Immaterial

AC TEST CIRCUITS AND WAVEFORMS

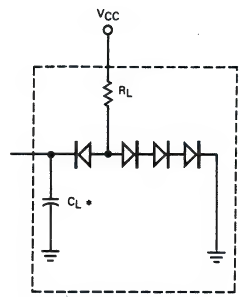
The following test circuits and conditions represent Fairchild's typical AC test procedures. The output loading for standard Low Power Schottky devices is a 15 pF capacitor. Experimental evidence shows that test results using the additional diode-resistor load are within 0.2 ns of the capacitor only load. The capacitor only load also has the advantage of repeatable, easily correlated test results. The input pulse rise and fall times are specified at 6 ns to closely approximate the Low Power Schottky output transitions through the active threshold region. The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

Test Circuit for Standard Output Devices

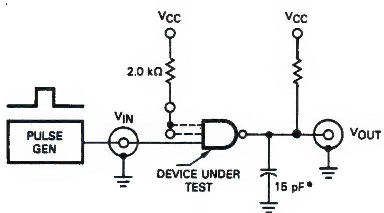


*Includes all probe and jig capacitance

Optional Load (Guaranted – Not Tested)



Test Circuit for Open Collector Output Devices

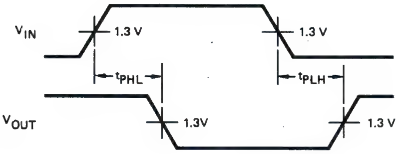


*Includes all probe and jig capacitance

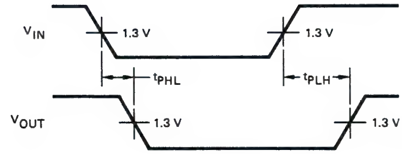
Pulse Generator Settings
(unless otherwise specified)

Frequency = 1 mHz
Duty Cycle = 50%
t_{TLH} (t_r) = 6 ns
t_{THL} (t_f) = 6 ns
Amplitude = 0 to 3 V

Waveform for Inverting Outputs



Waveform for Non-inverting Outputs



WAVEFORMS FOR 54LS/74LS73, LS74, LS76, LS78, LS107, LS109, LS112, LS113, LS114

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH

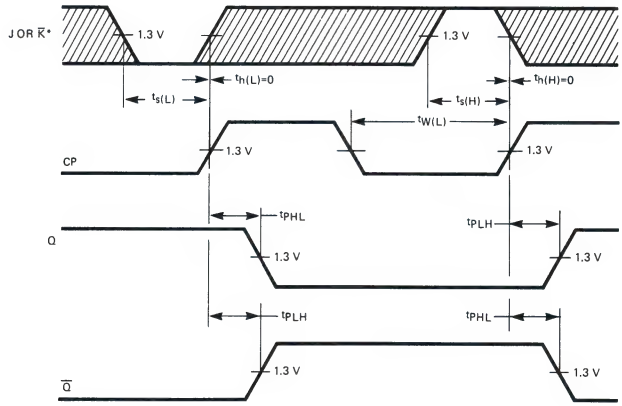


Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS

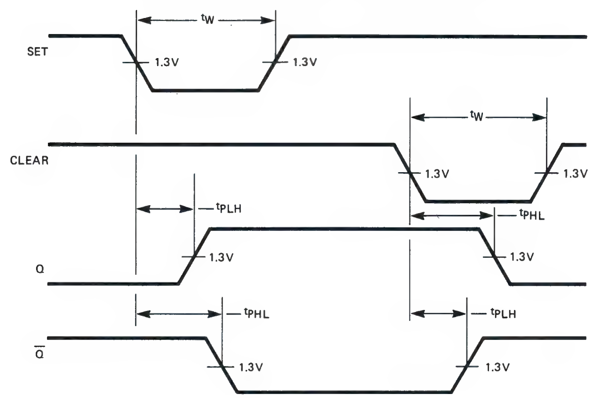
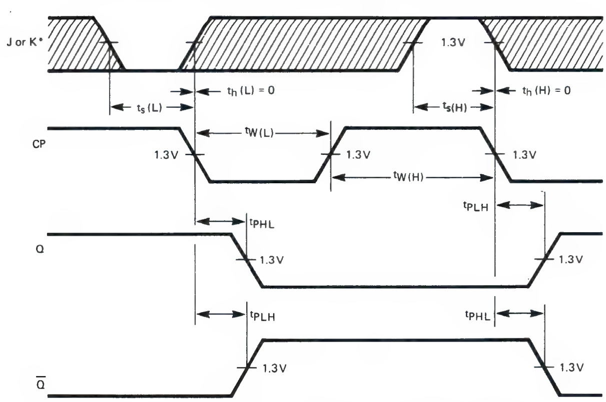


Fig. 3 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



*The shaded areas indicate when the input is permitted to change for predicatable output performance.

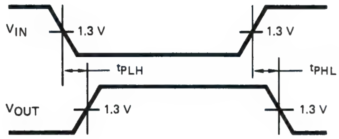


Fig. 1

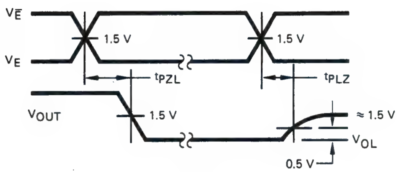


Fig. 2

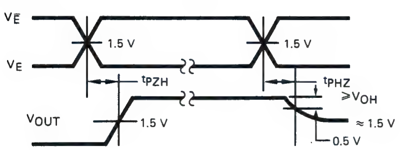


Fig. 3

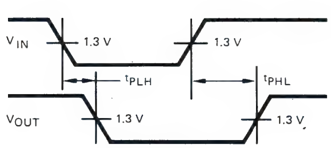


Fig. 4

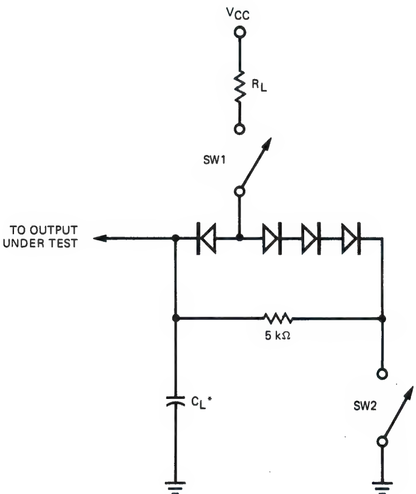
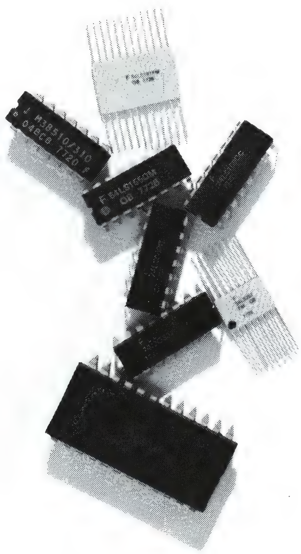


Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed



LOW POWER SCHOTTKY ORDERING INFORMATION

Fairchild digital integrated circuits may be ordered using a simplified purchasing code in which the package style and temperature range are defined below. Either the 74LS series number or the old 9LS series number may be used when ordering.

TEMPERATURE RANGE
M = Military -55°C to +125°C
C = Commercial 0°C to +70°C

PACKAGE STYLE

D = Dual In-Line — Ceramic (Hermetic)
P = Dual In-Line — Plastic
F = Flat Package

74LS00 D C

C — Temperature Range
D — Package Style
74LS00 — Device Type

In order to accommodate varying die sizes (SSI, MSI, etc.), numbers of pins (14, 16, 20, 24, etc.) and package outlines, a number of different package forms are required in each of the three package style categories.

The following lists indicate the specific package dimensions currently used for each device type. The detailed outline corresponding to each package code is shown at the end of this section.

LOW POWER SCHOTTKY
DEVICE MARKING EXAMPLE

74LS00
DC ⨍ Date Code

DEVICE	MILITARY (M) -55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS00	6A	3I	74LS00	6A	9A	3I
54LS02	6A	3I	74LS02	6A	9A	3I
54LS03	6A	3I	74LS03	6A	9A	3I
54LS04	6A	3I	74LS04	6A	9A	3I
54LS05	6A	3I	74LS05	6A	9A	3I
54LS08	6A	3I	74LS08	6A	9A	3I
54LS09	6A	3I	74LS09	6A	9A	3I
54LS10	6A	3I	74LS10	6A	9A	3I
54LS11	6A	3I	74LS11	6A	9A	3I
54LS13	6A	3I	74LS13	6A	9A	3I
54LS14	6A	3I	74LS14	6A	9A	3I
54LS15	6A	3I	74LS15	6A	9A	3I
54LS20	6A	3I	74LS20	6A	9A	3I
54LS21	6A	3I	74LS21	6A	9A	3I
54LS22	6A	3I	74LS22	6A	9A	3I
54LS26	6A	3I	74LS26	6A	9A	3I
54LS27	6A	3I	74LS27	6A	9A	3I

DEVICE	MILITARY (M) -55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS30	6A	3I	74LS30	6A	9A	3I
54LS32	6A	3I	74LS32	6A	9A	3I
54LS33	6A	3I	74LS33	6A	9A	3I
54LS37	6A	3I	74LS37	6A	9A	3I
54LS38	6A	3I	74LS38	6A	9A	3I
54LS40	6A	3I	74LS40	6A	9A	3I
54LS42	6B	4L	74LS42	6B	9B	4L
54LS47	6B	4L	74LS47	6B	9B	4L
54LS48	6B	4L	74LS48	6B	9B	4L
54LS49	6A	3I	74LS49	6A	9A	3I
54LS51	6A	3I	74LS51	6A	9A	3I
54LS54	6A	3I	74LS54	6A	9A	3I
54LS55	6A	3I	74LS55	6A	9A	3I
54LS73	6A	3I	74LS73	6A	9A	3I
54LS74	6A	3I	74LS74	6A	9A	3I
54LS75	6B	4L	74LS75	6B	9B	4L
54LS76	6B	4L	74LS76	6B	9B	4L
54LS77	6A	3I	74LS77	6A	9A	3I
54LS78	6A	3I	74LS78	6A	9A	3I
54LS83A	6B	4L	74LS83A	6B	9B	4L
54LS85	6B	4L	74LS85	6B	9B	4L
54LS86	6A	3I	74LS86	6A	9A	3I
54LS89	6B	4L	74LS89	6B	9B	4L
54LS90	6A	3I	74LS90	6A	9A	3I
54LS92	6A	3I	74LS92	6A	9A	3I
54LS93	6A	3I	74LS93	6A	9A	3I
54LS95B	6A	3I	74LS95B	6A	9A	3I
54LS107	6A	3I	74LS107	6A	9A	3I
54LS109	6B	4L	74LS109	6B	9B	4L
54LS112	6B	4L	74LS112	6B	9B	4L
54LS113	6A	3I	74LS113	6A	9A	3I
54LS114	6A	3I	74LS114	6A	9A	3I
54LS125	6A	3I	74LS125	6A	9A	3I
54LS126	6A	3I	74LS126	6A	9A	3I
54LS132	6A	3I	74LS132	6A	9A	3I
54LS133	6B	4L	74LS133	6B	9B	4L
54LS136	6A	3I	74LS136	6A	9A	3I
54LS138	6B	4L	74LS138	6B	9B	4L
54LS139	6B	4L	74LS139	6B	9B	4L
54LS145	6B	4L	74LS145	6B	9B	4L

DEVICE	MILITARY (M) -55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS151	6B	4L	74LS151	6B	9B	4L
54LS152		3I	74LS152			3I
54LS153	6B	4L	74LS153	6B	9B	4L
54LS155	6B	4L	74LS155	6B	9B	4L
54LS156	6B	4L	74LS156	6B	9B	4L
54LS157	6B	4L	74LS157	6B	9B	4L
54LS158	6B	4L	74LS158	6B	9B	4L
54LS160	6B	4L	74LS160	6B	9B	4L
54LS161	6B	4L	74LS161	6B	9B	4L
54LS162	6B	4L	74LS162	6B	9B	4L
54LS163	6B	4L	74LS163	6B	9B	4L
54LS164	6A	3I	74LS164	6A	9A	3I
54LS165	6B	4L	74LS165	6B	9B	4L
54LS168	6B	4L	74LS168	6B	9B	4L
54LS168	6B	4L	74LS168	6B	9B	4L
54LS169	6B	4L	74LS169	6B	9B	4L
54LS170	6B	4L	74LS170	6B	9B	4L
54LS173	6B	4L	74LS173	6B	9B	4L
54LS174	6B	4L	74LS174	6B	9B	4L
54LS175	6B	4L	74LS175	6B	9B	4L
54LS181	6N	4M	74LS181	6N	9N	4M
54LS182	6B	4L	74LS182	6B	9B	4L
54LS189	6B	4L	74LS189	6B	9B	4L
54LS191	6B	4L	74LS191	6B	9B	4L
54LS192	6B	4L	74LS192	6B	9B	4L
54LS193	6B	4L	74LS193	6B	9B	4L
54LS194	6B	4L	74LS194	6B	9B	4L
54LS195	6B	4L	74LS195	6B	9B	4L
54LS196	6A	3I	74LS196	6A	9A	3I
54LS197	6A	3I	74LS197	6A	9A	3I
54LS240	†	††	74LS240	†	9Z	††
54LS241	†	††	74LS241	†	9Z	††
54LS242	6A	3I	74LS242	6A	9A	3I
54LS243	6A	3I	74LS243	6A	9A	3I
54LS244	†	††	74LS244	†	9Z	††
54LS245	†	††	74LS245	†	9Z	††
54LS247	6B	4L	74LS247	6B	9B	4L
54LS248	6B	4L	74LS248	6B	9B	4L
54LS249	6B	4L	74LS249	6B	9B	4L
54LS251	6B	4L	74LS251	6B	9B	4L
54LS253	6B	4L	74LS253	6B	9B	4L
54LS257	6B	4L	74LS257	6B	9B	4L
54LS258	6B	4L	74LS258	6B	9B	4L
54LS259	6B	4L	74LS259	6B	9B	4L
54LS260	6A	3I	74LS260	6A	9A	3I
54LS266	6A	3I	74LS266	6A	9A	3I

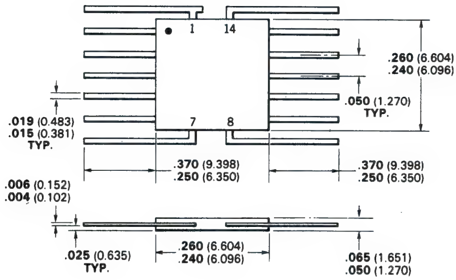
† No Ceramic 20 pin pkg. approved as of Sept. '77
†† No Flatpak 20 pin pkg. approved as of Sept. '77

DEVICE	MILITARY (M) -55°C to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54LS273	†	††	54LS273	†	9Z	††
54LS279	6B	4L	74LS279	6B	9B	4L
54LS283	6B	4L	74LS283	6B	9B	4L
54LS289	6B	4L	74LS289	6B	9B	4L
54LS290	6A	3I	74LS290	6A	9A	3I
54LS293	6A	3I	74LS293	6A	9A	3I
54LS295A	6A	3I	74LS295A	6A	9A	3I
54LS298	6B	4L	74LS298	6B	9B	4L
54LS299	†	††	74LS299	†	9Z	††
54LS323	†	††	74LS323	†	9Z	††
54LS352	6B	4L	74LS352	6B	9B	4L
54LS353	6B	4L	74LS353	6B	9B	4L
54LS365	6B	4L	74LS365	6B	9B	4L
54LS366	6B	4L	74LS366	6B	9B	4L
54LS367	6B	4L	74LS367	6B	9B	4L
54LS368	6B	4L	74LS368	6B	9B	4L
54LS373	†	††	74LS373	†	9Z	††
54LS374	†	††	74LS374	†	9Z	††
54LS375	6B	4L	74LS375	6B	9B	4L
54LS377	†	††	74LS377	†	9Z	††
54LS378	6B	4L	74LS378	6B	9B	4L
54LS379	6B	4L	74LS379	6B	9B	4L
54LS386	6A	3I	74LS386	6A	9A	3I
54LS390	6B	4L	74LS390	6B	9B	4L
54LS393	6B	4L	74LS393	6B	9B	4L
54LS395	6B	4L	74LS395	6B	9B	4L
54LS398	†	††	74LS398	†	9Z	††
54LS399	6B	4L	74LS399	6B	9B	4L
54LS490	6B	4L	74LS490	6B	9B	4L
54LS502	†	††	74LS502	†	9Z	††
54LS540	†	††	74LS540	†	9Z	††
54LS541	†	††	74LS541	†	9Z	††
54LS568	†	††	74LS568	†	9Z	††
54LS569	†	††	74LS569	†	9Z	††
54LS573	†	††	74LS573	†	9Z	††
54LS574	†	††	74LS574	†	9Z	††
54LS670	6B	4L	74LS670	6B	9B	4L
96L02	6B	4L	96L02	6B	9B	4L
96LS02	6B	4L	96LS02	6B	9B	4L
			96S02	6B	9B	4L
			96LS32	6N	9N	4M

† No Ceramic 20 pin pkg. approved as of Sept. '77
†† No Flatpak 20 pin pkg. approved as of Sept. '77

In Accordance with JEDEC TO-86 Outline 14-Pin Cerpak

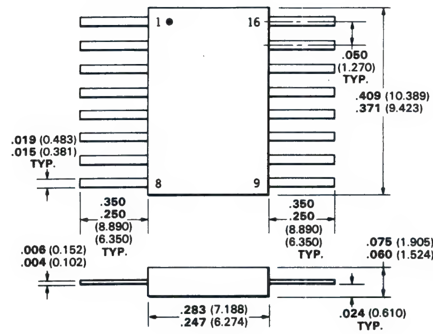
3I



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Package weight is 0.26 gram
Pin 1 orientation may be either tab or dot

16-Pin Cerpak

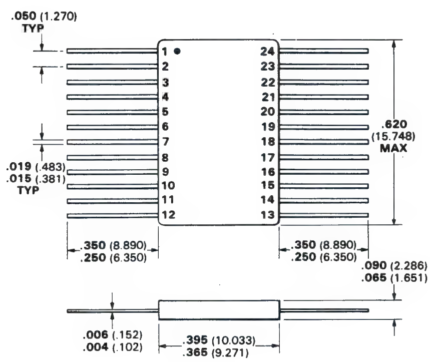
4L



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

24-Pin BeO Cerpak

4M

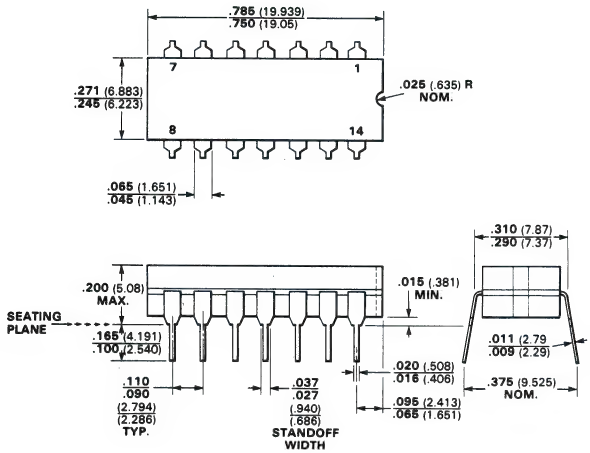


NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Package weight is 0.8 gram
Hermetically sealed beryllia package

6

In accordance with
JEDEC (TO-116) outline
14-Pin Ceramic Dual In-Line

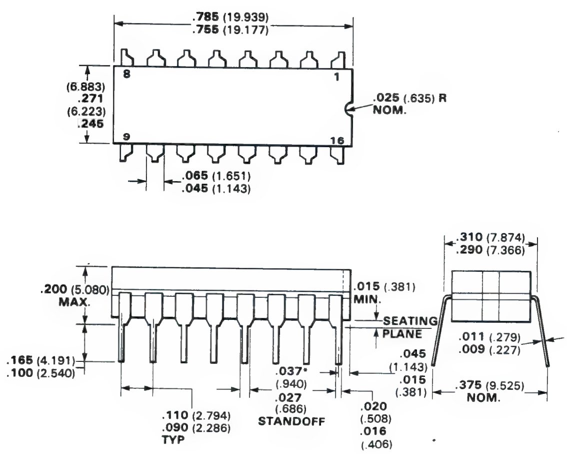
6A



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

16-Pin Ceramic Dual In-Line

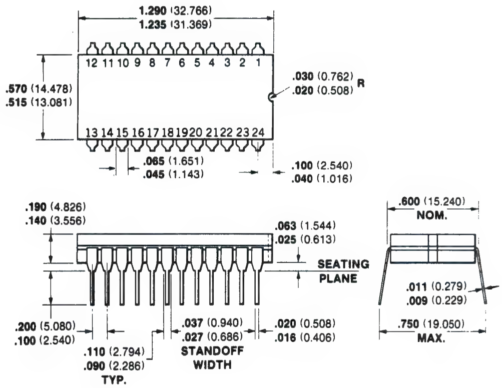
6B



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams
*The .037/.027 (.940/.686) dimensions does not apply to the corner pins

24-Pin Ceramic Dual In-Line

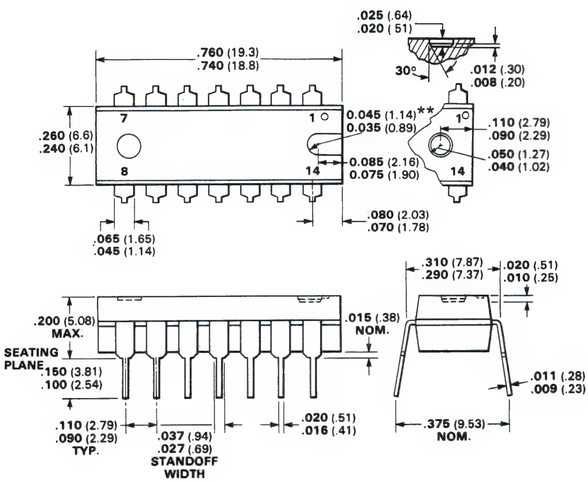
6N



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .600" (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Pins are alloy 42
Package weight is 6.5 grams
Package material is alumina

14-Pin Plastic Dual In-Line

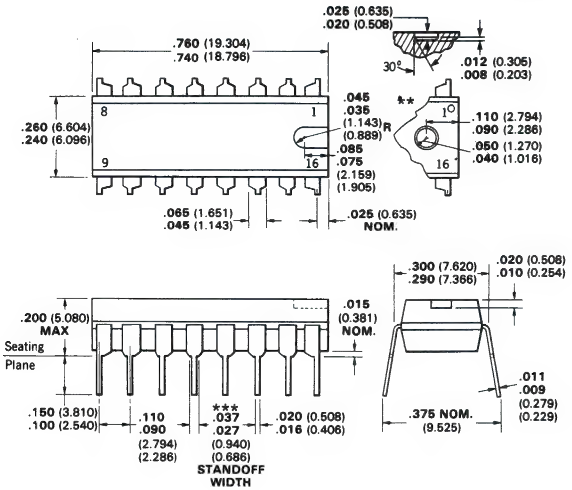
9A



NOTES:
All dimensions in inches (bold) and millimeters (parantheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
Pins are alloy 42
Package weight is 0.9 gram
Package material is silicone

16-Pin Plastic Dual In-Line

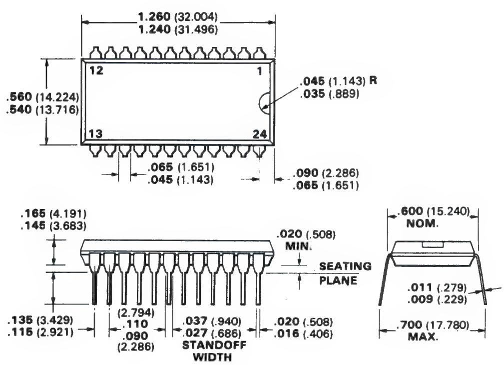
9B



NOTES:
- All dimensions in inches (bold) and millimeters (parentheses)
- Pins are alloy 42
- Pins are intended for insertion in hole rows on .300" (7.620) centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
- ***The .037/.027 (.940/.686) dimension does not apply to the corner pins
- Package weight is 0.9 gram

24-Pin Plastic Dual In-Line

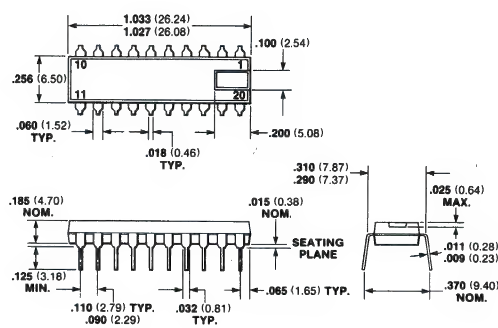
9N



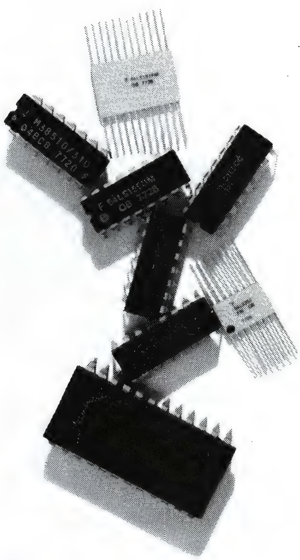
NOTES:
- All dimensions in inches (bold) and millimeters (parentheses)
- Pins are intended for insertion in hole rows on .600" (15.24) centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
- Pins are alloy 42

20-Pin Plastic Dual In-line

9Z



NOTES:
- All dimensions in inches (bold) and millimeters (parentheses)
- Pins are tin plated alloy 42 or copper (olin 195)
- Package material varies depending on the product line
- Pins are intended for insertion in hole rows on .300 (077.62) centers
- They are purposely shipped with "positive misalignment to facilitate insertion
- Board drilling dimensions should equal your practive for .020" (0.51) diameter pin
- Package weight is a little over 1.0 grams



FAIRCHILD FRANCHISED DISTRIBUTORS UNITED STATES AND CANADA

ALABAMA

HALLMARK ELECTRONICS
4739 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-8700 TWX: 810-726-2187

HAMILTON/AVNET ELECTRONICS
805 Oster Drive, N.W.
Huntsville, Alabama 35805
Tel: 205-533-1170
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

ARIZONA

HAMILTON/AVNET ELECTRONICS
2615 S. 21st Street
Phoenix, Arizona 85034
Tel: 602-275-7851 TWX: 910-951-1535

LIBERTY ELECTRONICS/ARIZONA
3130 N. 27th Avenue
Phoenix, Arizona 85016
Tel: 602-257-1272 TWX: 910-951-4282

STERLING ELECTRONICS
P.O. Drawer 20867 (zip code 85036)
2001 E. University Drive
Phoenix, Arizona 85034
Tel: 602-258-4531 Telex: 667317

CALIFORNIA

AVNET ELECTRONICS
350 McCormick Avenue
Costa Mesa, California 92626
Tel: 714-754-6111 (Orange County)
213-558-2345 (Los Angeles)
TWX: 910-595-1928

BELL INDUSTRIES
Electronic Distributor Division
1161 N. Fair Oaks Avenue
Sunnyvale, California 94086
Tel: 408-734-8570 TWX: 910-339-9378

ELMAR ELECTRONICS
2288 Charleston Rd.
Mountain View, California 94042
Tel: 415-961-3611 TWX: 910-379-6437

G.S. MARSHALL COMPANY
8005 Deering Avenue
Canoga Park, California 91304
Tel: 213-999-5001

G.S. MARSHALL COMPANY
9674 Telstar Avenue
El Monte, California 91731
Tel: 213-686-0141 TWX: 910-587-1565

G.S. MARSHALL COMPANY
17975 Skypark Blvd.
Irvine, California 92707
Tel: 714-556-6400

G.S. MARSHALL COMPANY
8057 Raytheon Rd. Suite 1
San Diego, California 92111
Tel: 714-278-6350 TWX: 910-335-1191

HAMILTON ELECTRO SALES
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

HAMILTON/AVNET ELECTRONICS
575 E. Middlefield Road
Mountain View, California 94040
Tel: 415-961-7000 TWX: 910-379-6486

HAMILTON/AVNET ELECTRONICS
8917 Complex Drive
San Diego, California 92123
Tel: 714-279-2421
Telex HAMAVELEC SDG 69-5415

LIBERTY ELECTRONICS
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

LIBERTY ELECTRONICS/SAN DIEGO
8248 Mercury Court
San Diego, California 92111
Tel: 714-565-9171 TWX: 910-335-1590

COLORADO

CENTURY ELECTRONICS
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel. 303-424-1985 TWX: 910-938-0393

CRAMER ELECTRONICS
5465 East Evans Place at Hudson
Denver, Colorado 80222
Tel: 303-758-2100

ELMAR ELECTRONICS
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

G.S. MARSHALL COMPANY
5633 Kendall Court
Arvada, Colorado 80002
Tel: 303-423-9670 TWX: 910-938-2902

HAMILTON/AVNET ELECTRONICS
5921 N. Broadway
Denver, Colorado 80216
Tel: 303-534-1212 TWX: 910-931-0510

CONNECTICUT

CRAMER ELECTRONICS
35 Dodge Avenue
Wharton Brook Industrial Center
North Haven, Connecticut 06473
Tel: 203-239-5641

HAMILTON/AVNET ELECTRONICS
643 Danbury Road
Georgetown, Connecticut 06829
Tel: 203-762-0361
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.)

HARVEY ELECTRONICS
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

SCHWEBER ELECTRONICS
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

FLORIDA

CRAMER ELECTRONICS
4035 N. 29th Avenue
Hollywood, Florida 33020
Tel: 305-923-8181

CRAMER ELECTRONICS
345 North Graham Avenue
Orlando, Florida 32814
Tel: 305-894-1511

HALLMARK ELECTRONICS
1302 W. McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

HALLMARK ELECTRONICS
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

HAMILTON/AVNET ELECTRONICS
6800 N.W. 20th Avenue
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-954-9808

SCHWEBER ELECTRONICS
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

GEORGIA

HAMILTON/AVNET ELECTRONICS
6700 Interstate 85 Access Raod, Suite 1E
Norcross, Ga. 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73 0511
(Regional Hq. in Dallas, Texas)

LYKES ELECTRONICS CORP.
6447 Atlantic Blvd.
Norcross, Georgia 30071
Tel: 404-449-9400

ILLINOIS

HALLMARK ELECTRONICS INC.
180 Crossen Avenue
Elk Grove Village, Illinois 60007
Tel: 312-437-8800

HAMILTON/AVNET ELECTRONICS
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

KIERULFF ELECTRONICS
85 Gordon Street
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

SCHWEBER ELECTRONICS, INC.
1275 Bummel Avenue
Elk Grove Village, Ill. 60007
Tel: 312-593-2740 TWX: 910-222-3453

SEMICONDUCTOR SPECIALISTS, INC
(mailing address)
O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666

(shipping address)
195 Spangler Avenue
Elmhurst Industrial Park
Elmhurst, Illinois 60126
Tel: 312-279-1000 TWX: 910-254-0169

INDIANA

GRAHAM ELECTRONICS SUPPLY, INC.
133 So. Pennsylvania Street
Indianapolis, Indiana 46204
Tel: 317-634-8486 TWX: 810-341-3481

PIONEER INDIANA ELECTRONICS, INC.
6408 Castleplace Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

KANSAS

HALLMARK ELECTRONICS, INC.
11870 West 91st Street
Shawnee Mission, Kansas 66214
Tel: 913-888-4746

HAMILTON/AVNET ELECTRONICS
37 Lenexa Industrial Center
9900 Pflumm Road
Lenexa, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

LOUISIANA

STERLING ELECTRONICS CORP.
4613 Fairfield
Metairie, Louisiana 70002
Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

MARYLAND

HALLMARK ELECTRONICS, INC.
6655 Amberton Drive
Baltimore, Maryland 21227
Tel: 301-796-9300

HAMILTON/AVNET ELECTRONICS
(mailing address)
Friendship International Airport
P.O. Box 8647
Baltimore, Maryland 21240

(shipping address)
7235 Standard Drive
Hanover, Maryland 21076
Tel: 301-796-5000 TWX: 710-862-1861
Telex: HAMAVLECA HNVE 87-968

PIONEER WASHINGTON ELECTRONICS, INC.
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX: 710-828-9784

SCHWEBER ELECTRONICS
5640 Fisher Lane
Rockville, Maryland 20852
Tel: 301-881-2970 TWX: 710-828-0536

MASSACHUSETTS

CRAMER ELECTRONICS
85 Wells Avenue
Newton Centre, Massachusetts 02159
Tel: 617-964-4000

GERBER ELECTRONICS
852 Providence Highway
U.S. Route 1
Dedham, Massachusetts 02026
Tel: 617-329-2400

HAMILTON/AVNET ELECTRONICS
100 E. Commerce Way
Woburn, Massachusetts 01801
Tel: 617-933-8000 TWX: 710- 332-1201

HARVEY ELECTRONICS
44 Hartwell Ave.
Lexington, Massachusetts 02173
Tel: 617-861-9200 TWX: 710-326-6617

SCHWEBER ELECTRONICS
213 Third Avenue
Waltham, Massachusetts 02154
Tel: 617-890-8484

MICHIGAN
HAMILTON/AVNET ELECTRONICS
12870 Farmington Rd.
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

PIONEER/DETROIT
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800

SCHWEBER ELECTRONICS
86 Executive Drive
Troy, Michigan 48084
Tel. 313-583-9242

SHERIDAN SALES CO.
24543 Indoplex Drive
(P.O. Box 529)
Farmington, Mich. 48024
Tel. 313-477-3800

MINNESOTA
HAMILTON/AVNET ELECTRONICS
7683 Washington Ave. South
Edina, Minnesota 55435
Tel. 612-941-3801
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

SCHWEBER ELECTRONICS
7402 Washington Ave. South
Eden Prairie, Minnesota 55343
Tel: 612-941-5280

SEMICONDUCTOR SPECIALISTS, INC.
8030 Cedar Avenue South
Minneapolis, Minnesota 55420
Tel. 612-854-8841 TWX: 910-576-2812

MISSOURI
HALLMARK ELECTRONICS, INC.
13789 Rider Trail
Earth City, Missouri 63045
Tel. 314-291-5350

HAMILTON/AVNET ELECTRONICS
364 Brookes Lane
Hazelwood, Missouri 63042
Tel: 314-731-1144 TWX: 910-762-0606

NEW JERSEY
HAMILTON/AVNET ELECTRONICS
218 Little Falls Road
Cedar Grove, New Jersey 07009
Tel. 201-239-0800 TWX: 710-994-5787

HAMILTON/AVNET ELECTRONICS
113 Gaither Drive
East Gate Industrial Park
Mt. Laurel, N.J. 08057
Tel. 609-234-2133 TWX: 710-897-1405

SCHWEBER ELECTRONICS
43 Belmont Drive
Somerset, N.J. 08873
Tel. 201-469-6008 TWX: 710-480-4733

STERLING ELECTRONICS
774 Pfeiffer Blvd.
Perth Amboy, N.J. 08861
Tel. 201-442-8000 Telex: 138-679

WILSHIRE ELECTRONICS
855 Industrial Highway, Unit 5
Cinnaminson, New Jersey 08077
Tel: 215-627-1920

WILSHIRE ELECTRONICS
1111 Paulison Avenue
Clifton, New Jersey 07011
Tel: 201-365-2600 TWX: 710-989-7052

NEW MEXICO
CENTURY ELECTRONICS
121 Elizabeth, N.E.
Albuquerque, New Mexico 87123
Tel. 505-292-2700 TWX: 910-989-0625

HAMILTON/AVNET ELECTRONICS
2450 Baylor Dr. S.E.
Albuquerque, New Mexico 87119
Tel. 505-765-1500
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

NEW YORK
CRAMER ELECTRONICS
129 Oser Avenue
Hauppauge, N.Y. 11787
Tel. 516-231-5682

CRAMER ELECTRONICS
6716 Joy Road
E. Syracuse, N.Y. 13057
Tel: 315-437-6671

COMPONENTS PLUS, INC.
40 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

HAMILTON/AVNET ELECTRONICS
167 Clay Road
Rochester, New York 14623
Tel: 716-442-7820
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Ma.)

HAMILTON/AVNET ELECTRONICS
6500 Joy Road
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

HAMILTON/AVNET ELECTRONICS
70 State Street
Westbury, L.I., New York 11590
Tel: 516-333-5800 TWX: 510-222-8237

ROCHESTER RADIO SUPPLY CO., INC.
140 W. Main Street
(P.O. Box 1971)
Rochester, New York 14603
Tel: 716-454-7800

SCHWEBER ELECTRONICS
Jericho Turnpike
Westbury, L.I.,New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

SCHWEBER ELECTRONICS, INC.
2 Town Line Circle
Rochester, New York 14623
Tel: 716-461-4000

JACO ELECTRONICS, INC.
145 Oser Ave.
Hauppauge, L.I.,New York 11787
Tel: 516-273-1234 TWX: 510-227-6232

SUMMIT DISTRIBUTORS, INC.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

NORTH CAROLINA
CRAMER ELECTRONICS
938 Burke Street
Winston Salem, N.C. 27102
Tel: 919-725-8711

HALLMARK ELECTRONICS
1208 Front Street, Bldg. K
Raleigh, North Carolina 27609
Tel: 919-832-4465 TWX: 510-928-1831

KIRKMAN ELECTRONICS, INC.
901 W. Second Street
Winston Salem, North Carolina 27108
Tel: 919-722-9131

PIONEER/CAROLINA ELECTRONICS
2906 Baltic Avenue
Greensboro, North Carolina 27406
Tel: 919-273-4441

OHIO
HAMILTON/AVNET ELECTRONICS
761 Beta Drive, Suite E
Cleveland, Ohio 44143
Tel: 216-461-1400
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

HAMILTON/AVNET ELECTRONICS
118 Westpark Road
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

PIONEER/CLEVELAND
4800 East 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

PIONEER/DAYTON
1900 Troy Street
Dayton, Ohio 45404
Tel: 513-236-9900 TWX: 810-459-1622

SCHWEBER ELECTRONICS
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

SHERIDAN SALES COMPANY
23224 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-831-0130 TWX: 810-427-2957

SHERIDAN SALES CO.
(mailing address)
P.O. Box 37826
Cincinnati, Ohio 45222

(shipping address)
10 Knollcrest Drive
Reading, Ohio 45237
Tel: 513-761-5432 TWX: 810-461-2670

OKLAHOMA
HALLMARK ELECTRONICS
4846 South 83rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

RADIO INC. INDUSTRIAL ELECTRONICS
1000 South Main
Tulsa, Oklahoma 74119
Tel: 918-587-9123

PENNSYLVANIA
HALLMARK ELECTRONICS, INC.
458 Pike Road
Huntingdon Valley, Pennsylvania 19006
Tel: 215-355-7300 TWX: 510-667-1727

PIONEER/DELAWARE VALLEY ELECTRONICS
141 Gibraltar Road
Horsham, Pa. 19044
Tel: 609-541-1120 TWX: 510-665-6778

PIONEER ELECTRONICS, INC.
560 Alpha Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

SCHWEBER ELECTRONICS
101 Rock Road
Horsham, Pennsylvania 19044
Tel: 215-441-0600

SHERIDAN SALES COMPANY
1717 Penn Ave.
Suite 5009
Pittsburgh, Pennsylvania 15221
Tel: 412-244-1640

SOUTH CAROLINA
DIXIE ELECTRONICS, INC.
P.O. Box 408 (Zip Code 29202)
1900 Barnwell Street
Columbia, South Carolina 29201
Tel: 803-779-5332

TEXAS
ALLIED ELECTRONICS
401 East 8th Street
Fort Worth, Texas 76102
Tel: 817-336-5401

CRAMER ELECTRONICS
13740 Midway Road, Suite 700
Dallas, Texas 75240
Tel: 214-661-9300

HALLMARK ELECTRONICS
9333 Forest Lane
Dallas, Texas 75231
Tel: 214-231-6111

HALLMARK ELECTRONICS, INC.
8000 Westglen
Houston, Texas 77063
Tel: 713-781-6100

HAMILTON/AVNET ELECTRONICS
4445 Sigma Road
Dallas, Texas 75240
Tel: 214-661-8661
Telex: HAMAVLECB DAL 73-0511

HAMILTON/AVNET ELECTRONICS
3939 Ann Arbor
Houston, Texas 77042
Tel: 713-780-1771
Telex: HAMAVLECB HOU 76-2589

SCHWEBER ELECTRONICS, INC.
14177 Proton Road
Dallas, Texas 75240
Tel: 214-661-5010 TWX: 910-860-5493

SCHWEBER ELECTRONICS, INC.
7420 Harwin Drive
Houston, Texas 77036
Tel: 713-784-3600 TWX: 910-881-1109

STERLING ELECTRONICS
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 901-881-5042
Telex: STELECO HOUA 77-5299

UTAH
CENTURY ELECTRONICS
2258 South 2700 West
Salt Lake City, Utah 84119
Tel: 801-487-8551 TWX: 910-925-5686

HAMILTON/AVNET ELECTRONICS
1585 West 2100 South
Salt Lake City, Utah 84119
Tel: 801-972-2800
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

WASHINGTON
HAMILTON/AVNET ELECTRONICS
13407 Northrup Way
Bellevue, Washington 98005
Tel: 206-746-8750 TWX: 910-443-2449

LIBERTY ELECTRONICS
1750 132nd Ave. N.E.
Bellevue, Washington 98005
Tel: 206-453-8300 TWX: 910-444-1379

RADAR ELECTRIC CO., INC.
168 Western Avenue West
Seattle, Washington 98119
Tel: 206-282-2511 TWX: 910-444-2052

WISCONSIN
HAMILTON/AVNET ELECTRONICS
2975 Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510

MARSH ELECTRONICS, INC.
1563 South 101 Street
Milwaukee, Wisconsin 53214
Tel: 414-475-6000

SEMICONDUCTOR SPECIALISTS, INC.
10855 W. Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-257-1330 TWX: 910-262-3022

CANADA
CAM GARD SUPPLY LTD.
640 42nd Avenue S.E.
Calgary, Alberta, T2G 1Y6, Canada
Tel. 403-287-0520 Telex: 03-822811

CAM GARD SUPPLY LTD.
10505 111th Street
Edmonton, Alberta T5H 3E8, Canada
Tel: 403-426-1805 Telex: 03-72960

CAM GARD SUPPLY LTD.
4910 52nd Street
Red Deer, Alberta, T4N 2C8, Canada
Tel: 403-346-2088

CAM GARD SUPPLY LTD.
825 Notre Dame Drive
Kamloops, British Columbia, V2C 5N8, Canada
Tel: 604-372-3338

CAM GARD SUPPLY LTD.
1777 Ellice Avenue
Winnepeg, Manitoba, R3H 0W5, Canada
Tel: 204-786-8401 Telex: 07-57622

CAM GARD SUPPLY LTD.
Rookwood Avenue
Fredericton, New Brunswick, E3B 4Y9, Canada
Tel: 506-455-8891

CAM GARD SUPPLY LTD.
15 Mount Royal Blvd.
Moncton, New Brunswick, E1C 8N6, Canada
Tel: 506-855-2200

CAM GARD SUPPLY LTD.
Courtenay Center.
Saint John, New Brunswick, E2L 2X6, Canada
Tel: 506-657-4666 Telex: 01-447489

CAM GARD SUPPLY LTD.
3065 Robie Street
Halifax, Nova Scotia, B3K 4P6, Canada
Tel: 902-454-8581 Telex: 01-921528

CAM GARD SUPPLY LTD.
1303 Scarth Street
Regina, Saskatchewan, S4R 2E7, Canada
Tel: 306-525-1317 Telex: 07-12667

CAM GARD SUPPLY LTD.
1501 Ontario Avenue
Saskatoon, Saskatchewan, S7K 1S7, Canada
Tel: 306-652-6424 Telex: 07-42825

ELECTRO SONIC INDUSTRIAL SALES
(TORONTO) LTD.
1100 Gordon Baker Rd.
Willowdale, Ontario, M2H 3B3, Canada
Tel: 416-494-1666
Telex: ESSCO TOR 06-22030

FUTURE ELECTRONICS CORPORATION
130 Albert Street
Ottawa, Ontario, K1P 5G4, Canada
Tel: 613-232-7757

FUTURE ELECTRONICS CORPORATION
44 Fasket Drive, Unit 24
Rexdale, Ontario, M9W IK5, Canada
Tel: 416-677-7820

FUTURE ELECTRONICS CORPORATION
5647 Ferrier Street
Montreal, Quebec, H4P 2K5, Canada
Tel: 514-735-5775

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
6291 Dorman Rd., Unit 16
Mississauga, Ontario, L4V 1H2, Canada
Tel: 416-677-7432 TWX: 610-492-8867

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
1735 Courtwood Crescent
Ottawa, Ontario, K1Z 5L9, Canada
Tel: 613-226-1700

HAMILTON/AVNET INTERNATIONAL
(CANADA) LTD.
2670 Paulus Street
St. Laurent, Quebec, H4S 1G2, Canada
Tel: 514-331-6443 TWX: 610-421-3731

R.A.E. INDUSTRIAL ELECTRONICS, LTD.
1629 Main Street
Vancouver, British Columbia, V6A 2W5, Canada
Tel: 604-687-2621 TWX: 610-929-3065
Telex: RAE-VCR 04-54550

SEMAD ELECTRONICS LTD.
625 Marshall Ave., Suite 2
Dorval, Quebec, H9P 1E1, Canada
Tel: 514-636-4614 TWX: 610-422-3048

SEMAD ELECTRONICS LTD.
1111 Finch Avech Ave. W., Suite 102
Downsview, Ontario, M3J 2E5, Canada
Tel: 416-635-9880 TWX: 610-492-2510

SEMAD ELECTRONICS LTD.
1485 Laperriere Ave.
Ottawa, Ontario, K1Z 7S8, Canada
Tel: 613-722-6571 TWX: 610-562-8966

FAIRCHILD SALES REPRESENTATIVES
UNITED STATES AND CANADA

ALABAMA
CARTWRIGHT & BEAN, INC.
2400 Bob Wallace Ave., Suite 201
Huntsville, Alabama 35805
Tel: 205-533-3509

CALIFORNIA
CELTEC COMPANY
2041 Business Center Drive, Suite 211
Irvine, California 92715
Tel: 714-752-6111 TWX: 910-595-2512

CELTEC COMPANY
15300 Ventura Blvd., Room 200
Sherman Oaks, California 91403
Tel: 213-990-3440 TWX: 910-495-2010

CELTEC COMPANY
7867 Convoy Court, Suite 312
San Diego, California 92111
Tel: 714-279-7961 TWX: 910-335-1512

MAGNA SALES, INC.
3212 Scott Blvd.
Santa Clara, California 95050
Tel: 408-985-1750 TWX: 910-338-0241

COLORADO
SIMPSON ASSOCIATES, INC.
2552 Ridge Road
Littleton, Colorado 80120
Tel: 303-794-8381 TWX: 910-935-0719

CONNECTICUT
PHOENIX SALES COMPANY
389 Main Street
Ridgefield, Connecticut 06877
Tel: 203-438-9644 TWX: 710-467-0662

FLORIDA
LECTROMECH, INC.
303 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-831-1577 TWX: 810-853-0262

LECTROMECH, INC.
2741 North 29th Avenue, Suite 218
Hollywood, Florida 33020
Tel: 305-920-2291 TWX: 510-954-9793

LECTROMECH, INC.
13519 88th Ave. North
Seminole, Florida 33542
Tel: 813-392-3172

GEORGIA
CARTWRIGHT & BEAN, INC.
P.O. Box 52846 (Zip Code 30355)
90 W. Wieuca Square, Suite 155
Atlanta, Georgia 30342
Tel: 404-255-5262 TWX: 810-751-3220

ILLINOIS
MICRO SALES, INC.
2258-B Landmeir Road
Elk Grove Village, Illinois 60007
Tel: 312-956-1000 TWX: 910-222-1833

INDIANA
LESLIE M. DEVOE COMPANY
7172 North Keystone Ave., Suite C
Indianapolis, Indiana 46240
Tel: 317-257-1227 TWX: 810-341-3284

IOWA
B.C. ELECTRONICS SALES, INC.
4403 First Avenue S.E., Suite 412
Cedar Rapids, Iowa 52402
Tel: 319-393-5818

KANSAS
B.C. ELECTRONIC SALES, INC.
P.O. Box 788
11495 Lenexa Drive
Olathe, Kansas 66061
Tel: 913-888-6680 TWX: 910-749-6414

MARYLAND
DELTA III ASSOCIATES
5801 Annapolis Road, Suite 500
Bladensburg, Maryland 20710
Tel: 301-779-0977 TWX: 710-826-9654

MASSACHUSETTS
SPECTRUM ASSOCIATES, INC.
888 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-2796 TWX: 710-348-0424

MICHIGAN
RATHSBURG ASSOCIATES
16621 E. Warren Ave.
Detroit, Michigan 48224
Tel: 313-882-1717 Telex: 23-5229

MINNESOTA
PSI COMPANY
7710 Computer Avenue
Minneapolis, Minnesota 55435
Tel: 612-835-1777 TWX: 910-576-3483

MISSISSIPPI
CARTWRIGHT & BEAN, INC.
P.O. Box 16728
5250 Galaxy Drive, Suite J
Jackson, Mississippi 39207
Tel: 601-981-1368

MISSOURI
B.C. ELECTRONIC SALES, INC.
300 Brookes Drive, Suite 105
Hazelwood, Missouri 63042
Tel: 314-731-1255 TWX: 910-762-0600

NEW JERSEY
LORAC SALES, INC.
580 Valley Road
Wayne, New Jersey 07470
Tel: 201-696-8875 TWX: 710-988-5846

NEW YORK
LORAC SALES, INC.
550 Old Country Road, Room 410
Hicksville, New York 11801
Tel: 516-681-8746 TWX: 510-224-6480

TRI-TECH ELECTRONICS, INC.
3215 East Main Street
Endwell, New York 13760
Tel: 607-754-1094 TWX: 510-252-0891

TRI-TECH ELECTRONICS, INC.
290 Perinton Hills Office Park
Fairport, New York 14450
Tel: 716-223-5720

TRI-TECH ELECTRONICS, INC.
6836 East Genesee Street
Fayetteville, New York 13066
Tel: 315-446-2881 TWX: 710-541-0604

TRI-TECH ELECTRONICS, INC.
15 College View Avenue
Poughkeepsie, New York 12603
Tel: 914-473-3880

NORTH CAROLINA
CARTWRIGHT & BEAN, INC.
1165 Commercial Ave.
Charlotte, North Carolina 28205
Tel: 704-377-5673

GARTWRIGHT & BEAN, INC.
P.O. Box 18465
3948 Browning Place
Raleigh, North Carolina 27609
Tel: 919-781-6560

OHIO
THE LYONS CORPORATION
4812 Frederick Road, Suite 105
Dayton, Ohio 45414
Tel: 513-278-0714

THE LYONS CORPORATION
6151 Wilson Mills Road, Suite 101
Highland Heights, Ohio 44143
Tel: 216-461-8288

OKLAHOMA
TECHNICAL MARKETING
9717 East 42nd Street, Suite 210
Tulsa, Oklahoma 74101
Tel: 918-622-5984

OREGON
QUADRA CORPORATION
P.O. Box 23681
4227 N.E. Azalea
Hillsboro, Oregon 97123
Tel: 503-225-0350 TWX: 910-443-2318

PENNSYLVANIA
BGR ASSOCIATES
2500 Office Center
2500 Maryland Road
Willow Grove, Pennsylvania 19090
Tel: 215-657-3301

TENNESSEE
CARTWRIGHT & BEAN, INC.
P.O. Box 4760
560 S. Cooper Street
Memphis, Tennessee 38104
Tel: 901-276-4442

CARTWRIGHT & BEAN, INC.
8501 Kingston Pike
Knoxville, Tennessee 37919
Tel: 615-693-7450

TEXAS
TECHNICAL MARKETING
4445 Alpha Road, Suite 102
Dallas, Texas 75240
Tel: 214-387-3601 TWX: 910-860-5158

TECHNICAL MARKETING
6430 Hillcroft, Suite 104
Houston, Texas 77036
Tel: 713-777-9228

UTAH
SIMPSON ASSOCIATES, INC.
P.O. Box 151430
Salt Lake City, Utah 84115
Tel: 801-486-3731

WASHINGTON
QUADRA CORPORATION
14825 N.E. 40th Street
Suite 340
Redmond, Washington 98052
Tel: 206-883-3550 TWX: 910-449-2592

WISCONSIN
LARSEN ASSOCIATES
10855 West Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-258-0529 TWX: 910-262-3160

CANADA
R.N. LONGMAN SALES, INC. (L.S.I.)
1590 Matheson Blvd, Unit 26-A
Mississauga, Ontario, L4W 1J1, Canada
Tel: 416-625-6770 TWX: 610-492-4311

R.N. LONGMAN SALES, INC. (L.S.I.)
1385 Mazurette Street West, Suite 3
Montreal, Quebec, H4N 1G8, Canada
Tel: 514-382-2552 TWX: 610-421-3178

FAIRCHILD SALES OFFICES
UNITED STATES AND CANADA

ALABAMA
Huntsville Office*
Executive Plaza
Suite 107
4717 University Drive, N.W.
Huntsville, Alabama 35805
Tel: 205-837-8960

ARIZONA
Phoenix Office
4414 N. 19th Avenue 85015
Suite G
Tel: 602-264-4948 TWX: 910-951-1544

CALIFORNIA
Los Angeles Office*
Crocker Bank Bldg.
15760 Ventura Blvd. Suite 1027
Encino 91436
Tel: 213-990-9800 TWX: 910-495-1776

Santa Ana Office*
2101 East Forth St. 92705
Bldg. B, Suite 185
Tel: 714-558-1881 TWX: 910-595-1109

Santa Clara Office*
3212-3214 Scott Blvd.
Santa Clara, 95050
Tel: 408-244-1400 TWX: 910-338-0241

FLORIDA
Ft. Lauderdale Office
Executive Plaza
Suite 300-B
1001 Northwest 62nd Street
Ft. Lauderdale, Florida 33309
Tel: 305-771-0320 TWX: 510-955-4098

Orlando Office*
Crane's Roost Office Park
303 Whooping Loop
Altamonte Springs 32701
Tel: 305-834-7000 TWX: 810-850-0152

GEORGIA
Atlanta Office*
1641 Wellshire Lane
Dunwoody, Ga. 30338
Tel: 404-394-5298

ILLINOIS
Chicago Office*
The Tower - Suite 610
Rolling Meadows 60008
Tel: 312-640-1000

INDIANA
Ft. Wayne Office
2118 Inwood Drive 46805
Suite 111
Tel: 219-483-6453 TWX: 810-332-1507

Indianapolis Office*
Room 205
7202 N. Shadeland 46250
Tel: 317-849-5412 TWX: 810-260-1793

KANSAS
Kansas City Office
Corporate Woods
10875 Grandview, Suite 2255
Overland Park 66210
Tel: 913-649-3974

MARYLAND
Bladensburg Office
5801 Annapolis Road 20710
Suite 500
Tel: 301-779-0954 TWX: 710-826-9654

MASSACHUSETTS
Boston Office*
888 Worcester Street
Wellesley Hills 02181
Tel: 617-237-3400 TWX: 710-348-0424

MICHIGAN
Detroit Office*
Johnston Building, Suite 24
20793 Farmington Road
Farmington Hills 48024
Tel: 313-478-7400 TWX: 810-242-2973

MINNESOTA
Minneapolis Office*
7600 Parklawn Avenue
Room 251
Edina 55435
Tel: 612-835-3322 TWX: 910-576-2944

NEW JERSEY
Wayne Office
580 Valley Road 07490
Suite 1
Tel: 201-696-7070

NEW MEXICO
Albuquerque Office
2403 San Mateo N.E. 87110
Plaza 13
Tel: 505-265-5601 TWX: 910-989-1186

NEW YORK
Melville Office*
275 Broadhollow Road 11746
Tel: 516-293-2900 TWX: 510-224-6480

Poughkeepsie Office
15 College View Ave. 12603
Tel: 914-452-4200 TWX: 510-248-0030

Rochester Office*
260 Perinton Hills Office Park
Fairport 14450
Tel: 716-223-7700

OHIO
Dayton Office
4812 Frederick Road 45414
Suite 105
Tel: 513-278-8278 TWX: 810-459-1803

OKLAHOMA
Tulsa Office
9717 E. 42nd Street 74101
Suite 210
Tel: 918-663-7131

PENNSYLVANIA
Philadelphia Office*
2500 Office Center
2500 Maryland Road
Willow Grove, Pa. 19090
Tel: 215-657-2711

TEXAS
Dallas Office*
13771 N. Central Expressway 75231
Suite 809
Tel: 214-234-3391 TWX: 910-867-4757

Houston Office*
6430 Hillcroft 77081
Suite 102
Tel: 713-771-3547 TWX: 910-881-6278

CANADA
Toronto Regional Office
Fairchild Semiconductor
1590 Matheson Blvd, Unit 26
Mississauga, Ontario L4W 1J1, Canada
Tel: 416-625-7070 TWX: 610-492-4311

INTERNATIONAL FAIRCHILD SALES OFFICES

AUSTRALIA
Fairchild Australia Pty Ltd.
72 Whiting Street
Artarmon 2064
New South Wales
Australia
Tel: Sydney (02)-438-2733

(mailing address)
P.O. Box 450
North Sydney 2060
New South Wales
Australia

AUSTRIA AND EASTERN EUROPE
Fairchild Electronics
A-1010 Wien
Schwedenplatz 2
Tel: 0222 63581 Telex: 75096

BRAZIL
Fairchild Semicondutores Ltda
Caixa Postal 30407
Rua Alagoas, 663
01242 Sao Paulo, Brazil
Tel: 66-9092 Telex: 011-23831
Cable: FAIRLEC

FRANCE
Fairchild Camera & Instrument S.A.
121, Avenue d'Italie
750013-Paris, France
Tel: 00331-504-5566 Telex: 0042 20614

GERMANY
Fairchild Camera and Instrument (Deutschland)
8046 Garching Hochbruck
Daimlerstr 15
Munich, Germany
Tel: (089) 320031 Telex: 52 4831 fair d

Fairchild Camera and Instrument (Deutschland)
3000 Hannover
Koenigsworther Strasse 23
Hanover, Germany
Tel: 0511 17844 Telex:09 22922

Fairchild Camera and Instrument (Deutschland)
7251 Leonberg
Poststrabe 37
Tel: 07152 41026 Telex: 07 245711

Fairchild Camera and Instrument (Deutschland)
85 Nuernberg
Waldluststrasse 1
Tel: 0911 407005 Telex: 06 23665

HONG KONG
Fairchild Semiconductor (HK) Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
Tel: K-890271 Telex: HKG-531

ITALY
Fairchild Semiconduttori, S.P.A.
Via Flamenia Vecchia 653
00191 Roma, Italy
Tel: 02 6887451 Telex: 36522

Fairchild Semiconduttori S.P.A.
Via Rosellini, 12
20124 Milano, Italy
Tel: 02 6887451 Telex: 36522

JAPAN
TDK-Fairchild
Asahi Seimei Shibuya Bldg. 2nd Floor
7-8 Shibuya, 1-Chrome
Shibuya-ku
Tokyo 150, Japan
Tel: 03 400 8351 Telex: 242173

KOREA
Fairchild Semikor Ltd.
551-1 Shin Dae Bank-Dong
Kwan Ak-Ku Seoul 151, Korea
Tel: 697741 & 691410 Telex: FAIRKOR 22705

(mailing address)
Central P.O. Box 2806

MEXICO
Fairchild Mexicana S.A.
Blvd. Adolfo Lopez Mateos No. 163
Mexico 19, D.F.
Tel: 905-563-5411 Telex: 017-71-038

SCANDINAVIA
Fairchild Semiconductor AB
Svartengsgatan 6
S-11620 Stockholm
Sweden
Tel: 8-449255 Telex: 17759

SINGAPORE
Fairchild Semiconductor Pty Ltd.
No. 11, Lorong 3
Toa Payoh
Singapore 12
Tel: 531-066 Telex: FAIRSIN-RS 21376

TAIWAN
Fairchild Semiconductor (Taiwan) Ltd.
Hsietsu Building, Room 502
47 Chung Shan North Road
Sec. 3 Taipei, Taiwan
Tel: 573205 thru 573207

BENELUX
Fairchild Semiconductor
Pradijslaan 39
Eindhoven, Holland
Tel: 0031-40446909 Telex: 00-1451024

UNITED KINGDOM
Fairchild Camera and Instrument (UK) Ltd.
Semiconductor Division
230 High Street
Potters Bar
Hertfordshire EN6 5BU
England
Tel: 0707 51111 Telex: 0051 262835

Fairchild Semiconductor Ltd.
Shiel House
Craigshill
Livingston
West Lothian, Scotland
Tel: Livingston 0589 32891 Telex: 72629

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

FAIRCHILD